5.7 Front-end electronics

5.7.1 Principle of operation

The choice of preamplifier configuration has to take into account the shape of the signal to be processed. The current signal has the shape $i_s(t)=i_o\exp(kt)$ ($0\leq t\leq 13$ ns, for $C_2H_2F_4$-based gas mixtures having drift speed in the order of 150 μ/ns) and comes from a strip-line whose characteristic impedance (for an RPC with 2-mm double-gap geometry and 2-4 cm strip width) ranges from 15 to 30 ohms.

With a suitable choice of the preamplifier time constant, either a current-mode ($v_o=Gi_s$) or a charge-mode configuration ($v_o=G\int i_s$) could be designed.

A current-mode amplifier requires a bandwidth of some hundreds of Mhz, in order to preserve the signal shape. This solution could be useful with a trailing-edge discriminator (the second edge of the signal is steeper than the first one, being it determined by the collection time of the electron cloud on the anode), or with a time-over-threshold discriminator (that carries out the average of timing taken on both edges). But these advantages are at least partially canceled by the amount of noise σ_n due to the large bandwidth. In fact, it is known that the timing error on a single threshold crossing is $\sigma_t=\sigma_n/(dv/dt)$, dv/dt being the signal slope around the threshold.

The situation appears more favorable with an amplifier working in charge mode. In fact, on one hand the leading-edge slope does not change, i_s being of exponential form. On the other hand the noise can be reduced by decreasing the bandwidth of the amplifier. The response will be a pulse having a long tail. Since the event rate at the amplifier input is less than 1 MHz (with the maximum strip area of 100x4 cm^2), a tail length in the order of many hundreds of ns is allowed. Thus, no further shaping is required. This architecture is particularly suitable with a leading-edge or a constant-fraction discriminator. However, it should be outlined that a constant-fraction comparator could hardly be integrated in a chip, being it difficult to make an analog delay of some tens of ns and being the dynamic range of the signals very large (the signal charge spans over 3-4 decades).

5.7.2 Electrical schematics

The front-end channel is made of a preamplifier, a discriminator-monostable and a driver. The preamplifier is made of a transresistance stage, to match the characteristic impedance of the strip. An exact matching whatever the signal charge can hardly be obtained: due to the wide dynamic range, a low power amplifier is soon overloaded. The impedance matching is important for small signals, around the threshold, where the reflections could affect the timing. On the other hand, looking at typical charge distributions of the detector, the probability of having charge signals below 50 fC is quite small. In the present version of the front-end, the input impedance is about 30 ohms.

The transresistance stage is followed by an integrator, that introduces the dominant pole at 16 MHz. The next high frequency pole (that must be as high as possible, in order that the pulse leading-edge be left unaffected) is set by the input stage and is 200 MHz. The charge sensitivity has been limited to 1.6 mV/fC, on the basis of our past experience on the detector. The ENC is 1.3 fC + 0.002fC/pF. The power consumption is 7 mW.

The comparator and the threshold circuit are made of many cascaded differential stages. The threshold can range between 10 and 300 fC, with an external voltage control.

The discriminator is followed by a one-shot circuit, that gives a pulse shaped at 150 nsec. The purpose of the monostable is to mask a possible streamer pulse that, sometimes, follows the proportional pulse within a delay ranging from 0 to some tens of ns.

The power consumption of the discriminator + monostable is 7 mW.

The driver has to fed a twisted pair cable with a signal level of 300 mV on 110 ohms, as required by receivers in LVDS technology. The corresponding power consumption is 18 mW. We are also considering the possibility of housing part of the readout

electronics on the same PCB of front-end. This solution would make the cable unnecessary, and the driver power could be decreased down to 5 mW. For this purpose, the chip has the possibility of reducing the driver output current.

Fig. 5.7.1, 5.7.2, 5.7.3 show the schematics of the circuits.

Fig. 5.7.4 shows the time slewing (simulated) introduced by the front-end channel as a function of charge overdrive. The nice performance of the comparator for overdrives down to 1 fC should be noted. The contribution of the preamplifier is due, as known, to the time the signal takes to reach the threshold. The upper limit expected for this delay is ~13 ns, corresponding to the electron drift time in a 2mm gap with a drift speed of 150 μ/ns.

Fig. 5.7.5 shows the simulated time resolution, obtained by weighting the time slewing with the probability of occurrence of each charge value. The value σ_t=0.67 nsec comes from having included into the simulation only the effect of amplitude variations of the amplifier signal. The real σ_t (measured with an amplifier in hybrid technology, similar to that of the chip, and with a LeCroy leading-edge discriminator) results to be 1.7 nsec. The difference should be attributed to the noise, both instrumental and pick-up, non included into the simulation.

5.7.3 Technology

In the present version, the front-end ASIC has been made in semi-custom bipolar technology by Maxim. This process has been already used in many high energy physics experiments, and its radiation hardness was considered adequate even at the deepest radiation levels of LHC.

The number of channels/chip was limited to 6, in order to optimize both the chip internal layout and the external connections to the strips.

The requested power supplies are +3V and -2V; the overall power consumption is around 30mW/channel.

The package is quad-flat-pack, 64 pins, 10x10 mm^2.

25 prototypes were just delivered, and we are about to start the bench tests and, successively, the tests on the detector.

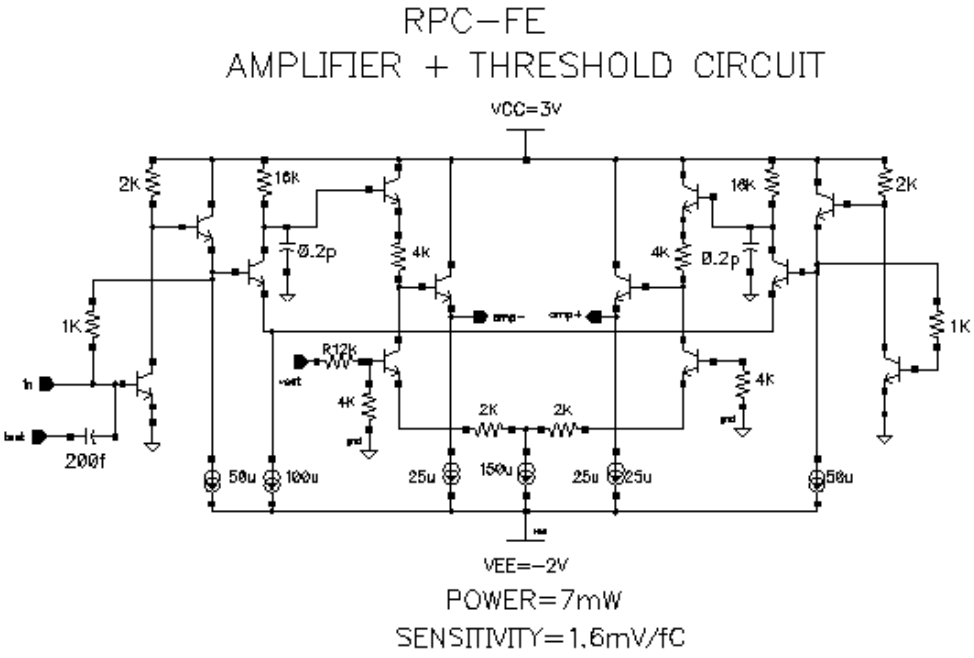

Fig. 5.7.1

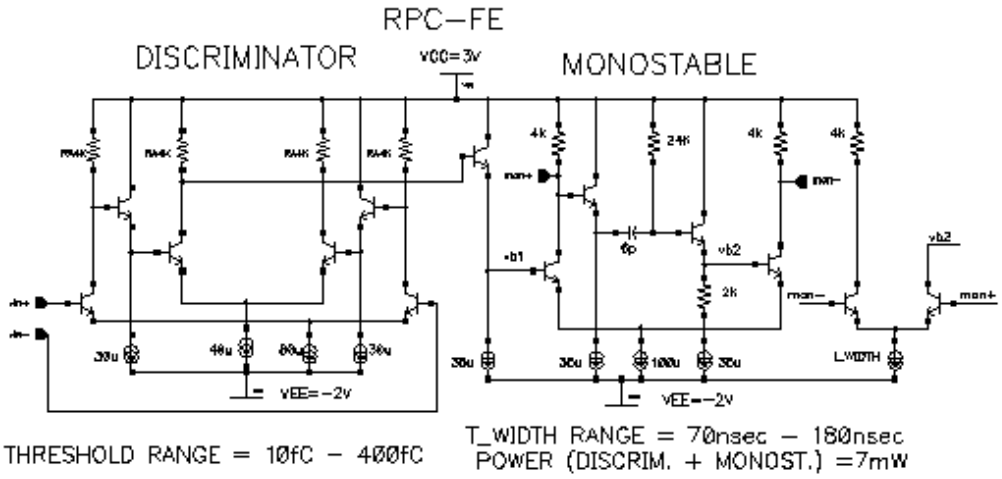

Fig. 5.7.2

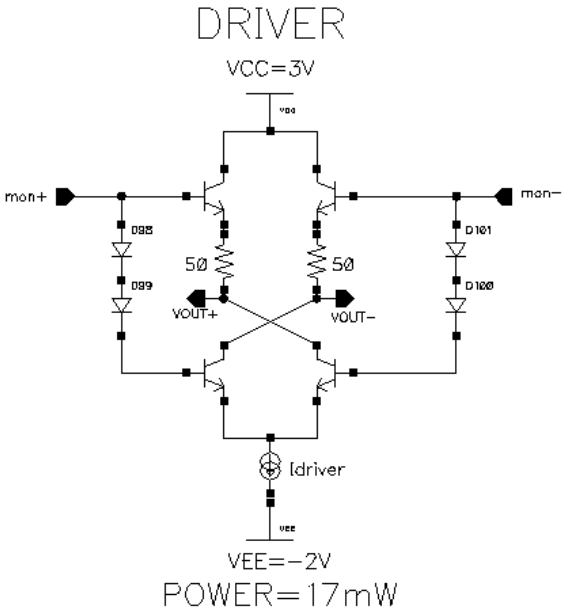

Fig. 5.7.3

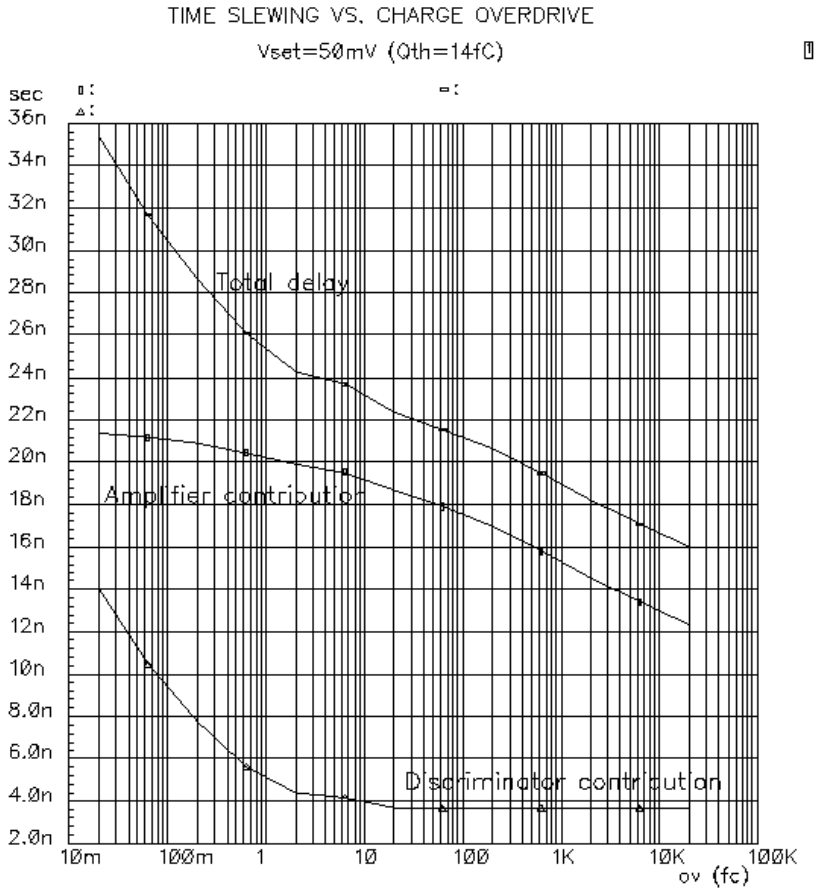

Fig. 5.7.4