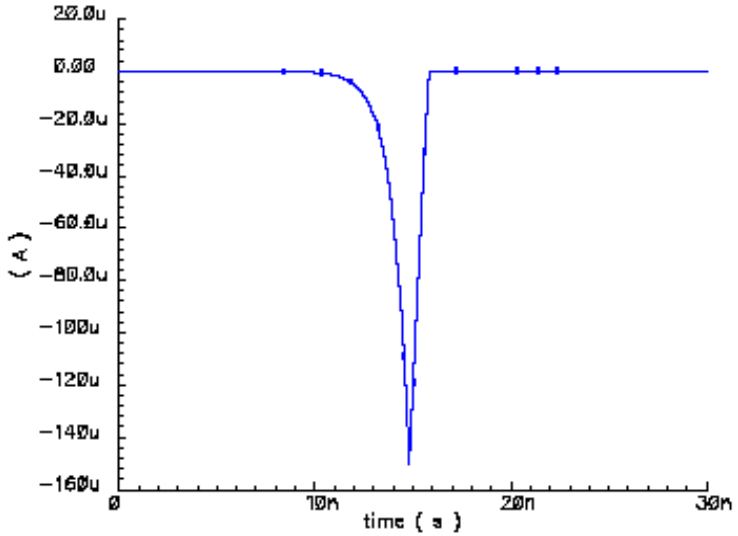
RPC Front End & Synchronization

- **RPC signal characteristics and FE electronics requirements**
- **FE electronics layout for synchronization**
- **Sources of RPC signal timing indetermination**
- **Results on last test beam data**
- **Results on laboratory FE board tests (Synchronizer)**
- **Conclusions: New Front End Chip & new FEB implementation**

RPC

Shape of the signal: $I(t) = I_0 \exp(t/\tau)$ $(0 \le t \le 15$ ns$)$

$\tau = 1/\eta v$ (~ 0.8 ns, at detector working point)



Strip line 1.3 m long and 2 - 4 cm wide:

$15\ \Omega \le R_0 \le 40\ \Omega$

160 pF $\le C_{strip} \le$ 350 pF

Propagation delay ~ 5.5 ns/m

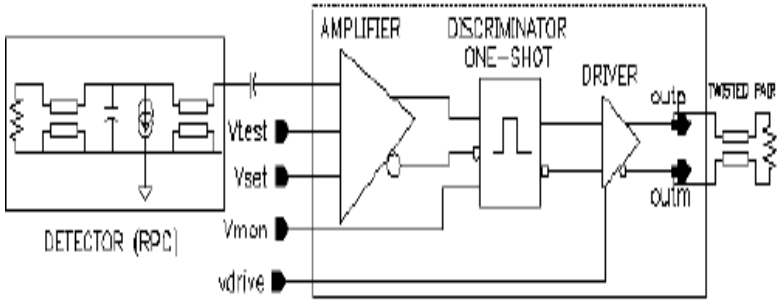
- **Input dynamic range:** 20 fC $\le Q_{in} \le$ 20 pC

- **Expected rate:** < 400 KHz

RPC Front-End chip (1997-1998)

RPC

•Shape of the signal: $I(t) = \exp(t/\tau)$ $(0 \le t \le 15$ ns)
•Strip line 1.3 m long and 2-4 cm wide:
$15\ \Omega \le R_0 \le 40\ \Omega$
160 pF $\le C_{strip} \le 350$ pF
Propagation delay ≈ 5.5 ns/m
•Input dynamic range: 20 fC $\le Q_{in} \le$ 20 pC

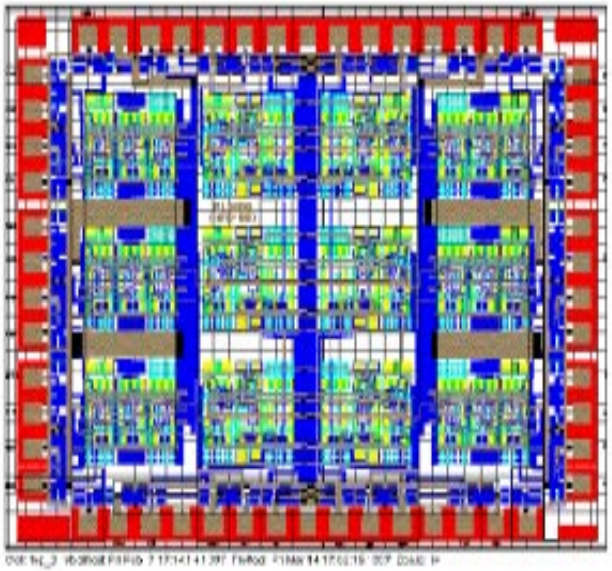


The circuit

Six channels, each one consisting of:
•charge amplifier
•leading-edge discriminator
•one-shot
•differential line driver

Amplifier characteristic:

•Current sensitive preamplifier:
$R_{in} = 30\ \Omega$ at the signal frequencies (100 MHz)
Dominant pole ~ 180 MHz
•Gain stage:
Dominant pole ~ 18 MHz
Charge sensitivity ~ 1.6 mV/fC
Power consumption ~ 7mW
ENC_{TOT} (strip connected and terminated) ≤ 1.6 fC



Discriminator + One-shot characteristics:

•10 fC $\le Q_{th} \le$ 300 fC
•70 ns $\le T_W \le$ 200 ns
•Power consumption ~ 7 mW

Output stage characteristics:

•Output Voltage swing: 0-300mV
•$R_O = 110\ \Omega$
•5mW (high impedance) $\le$ Power consumption $\le$ 17 mW (110 Ω)

RPC

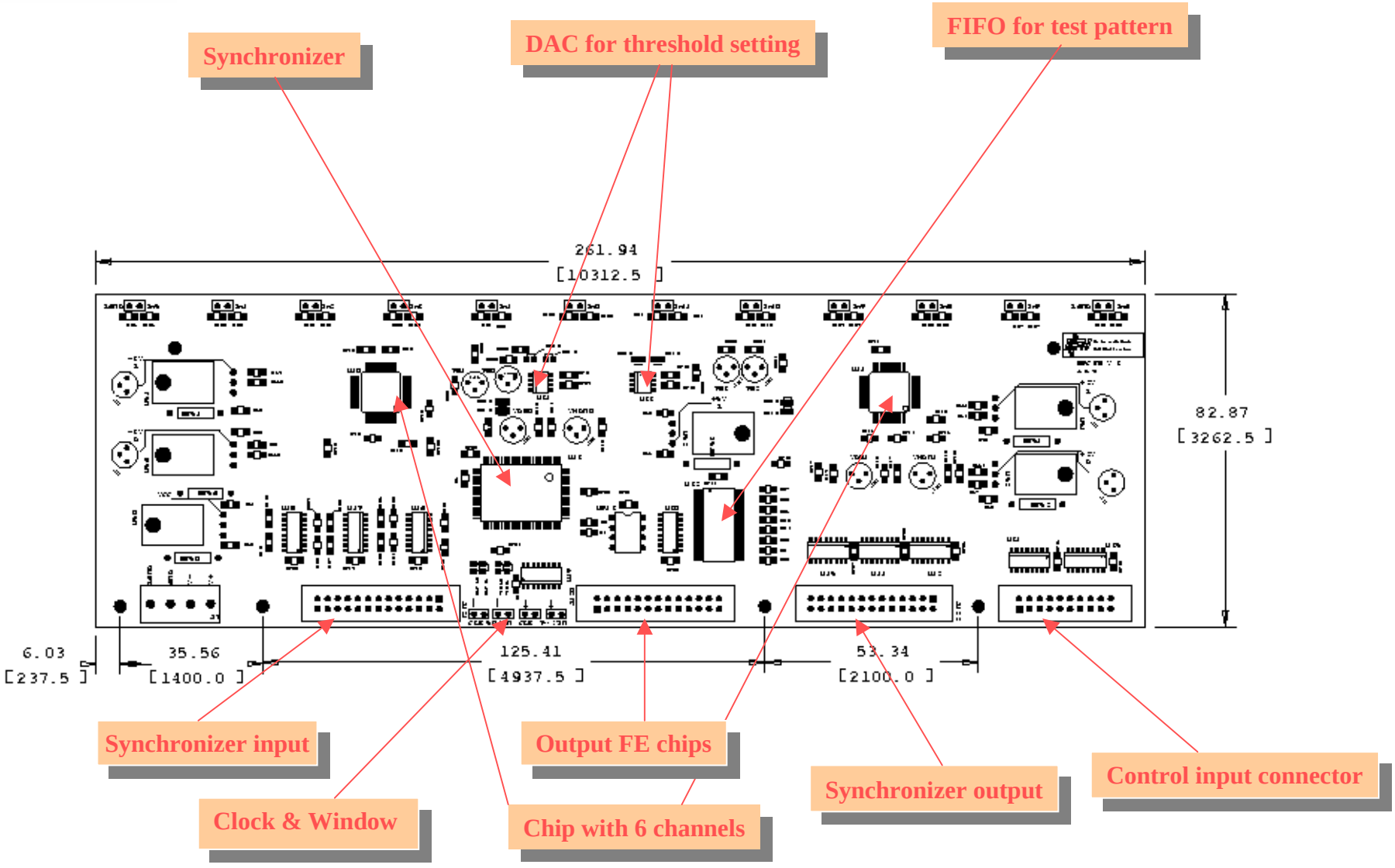
RPC Front_End board components

(1998 Test Beam implementation)

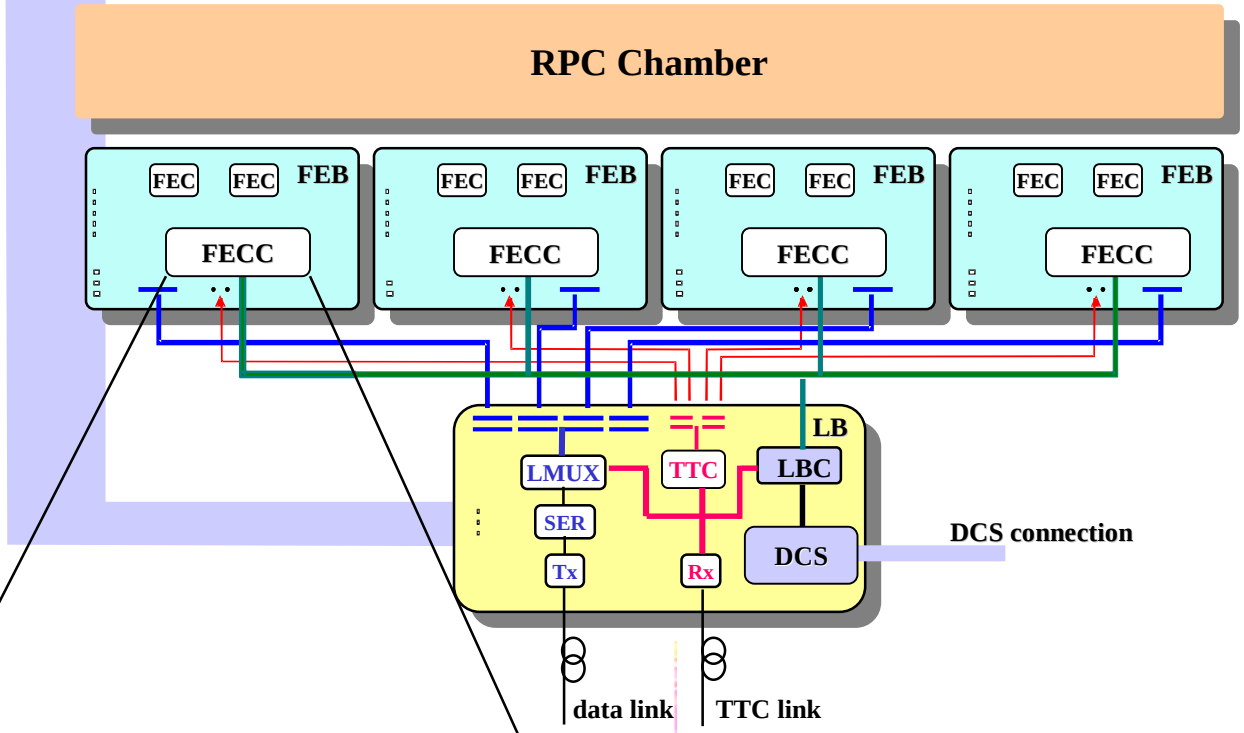
- **Modularity: 12 channels**
- **Front_End chip (Amplifier, Discriminator, One_Shot, Driver)**
- **Front_End Control Electronics:**
  - **DAC (threshold settings, 1.2 fC resolution)**
  - **FIFO for test pattern (512 x 18 bit word)**
  - **Synchronization Unit (window: position and width)**
  - **40 MHz clock**
- **LVDS output driver**
- **NIM module for remote control (present implementation)**

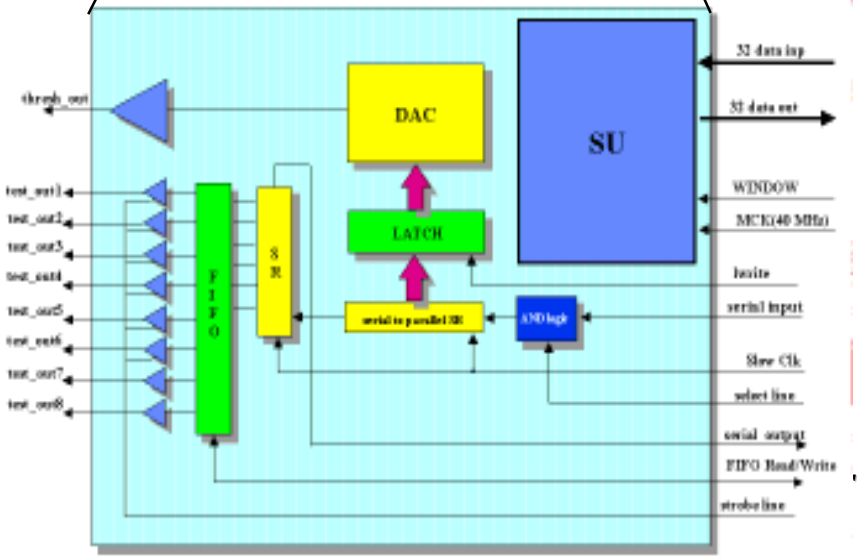
RPC

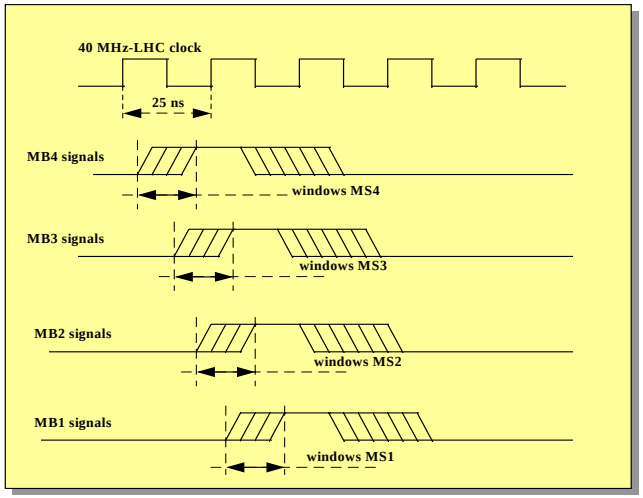
RPC Fron End Board Layout (1998)



RPC Front End & Synchronization Layout

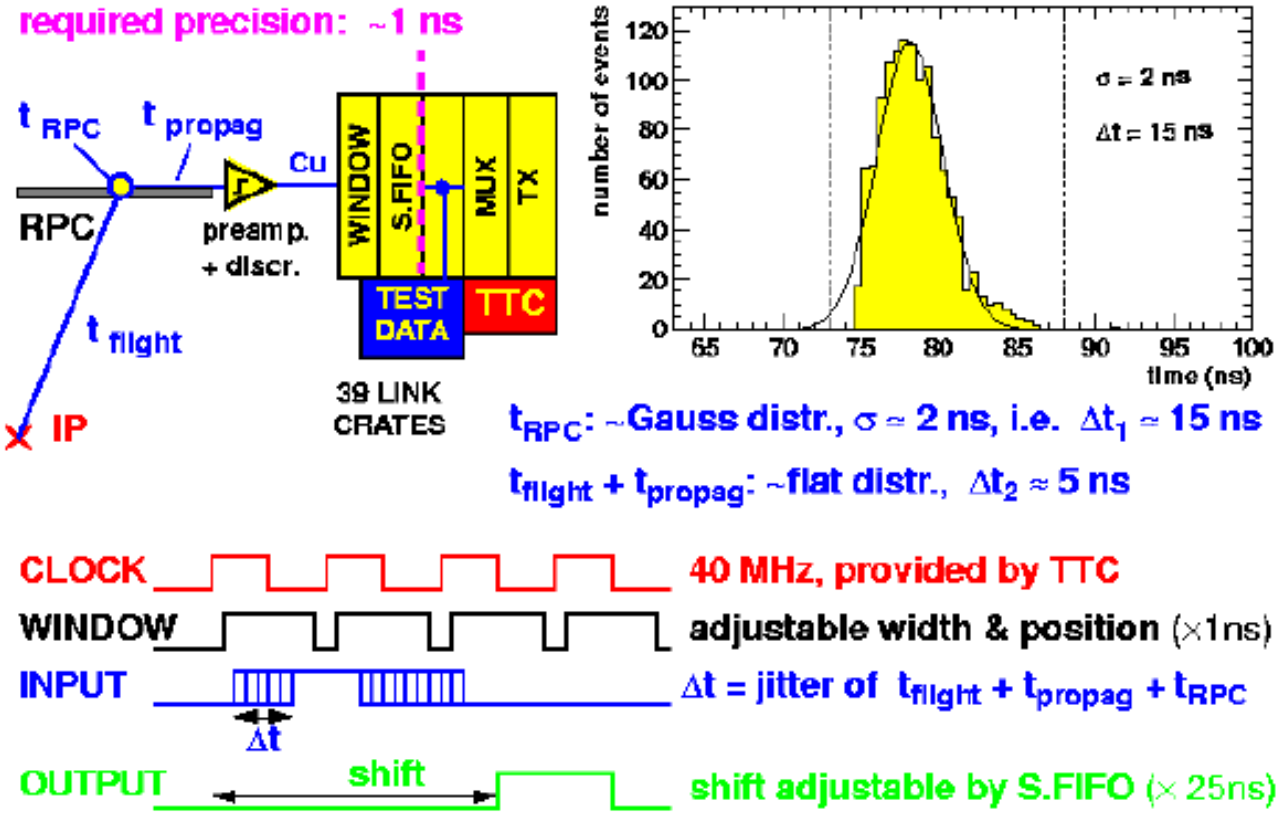






RPC

Alignment of RPC signals

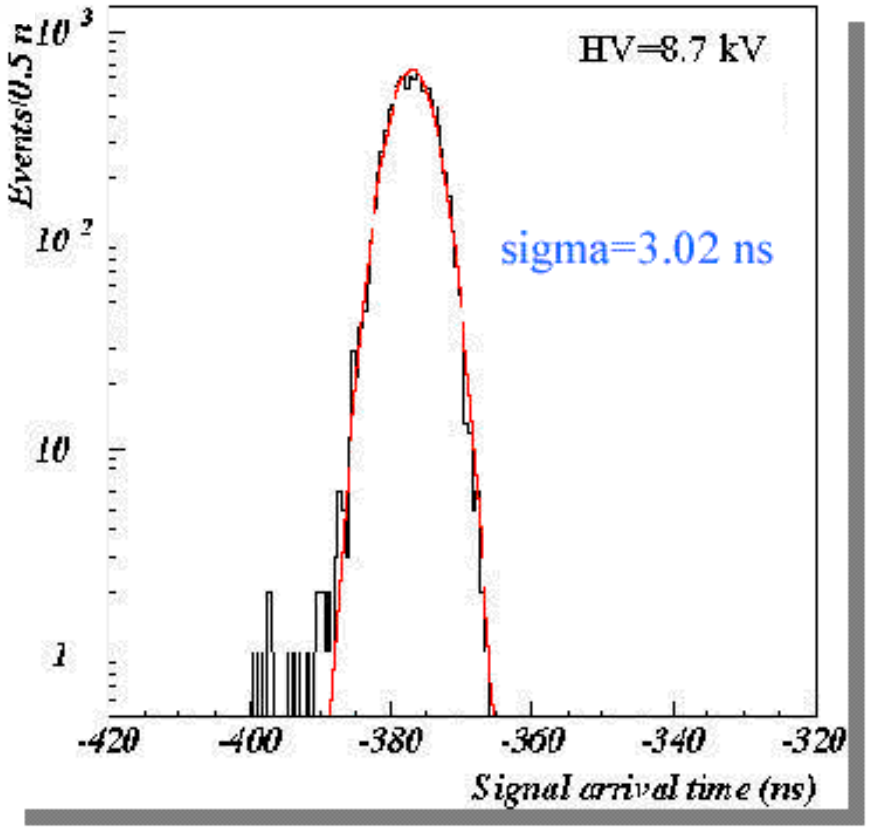


t_{RPC}: ~Gauss distr., $\sigma \simeq 2$ ns, i.e. $\Delta t_1 \simeq 15$ ns

$t_{flight} + t_{propag}$: ~flat distr., $\Delta t_2 \simeq 5$ ns

RPC

Signal arrival time distribution (arbitrary zero)



The tail on the left hand side is consistent with the background due to the spurious.

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Corrected signal arrival time distribution for a 2 mm RPC

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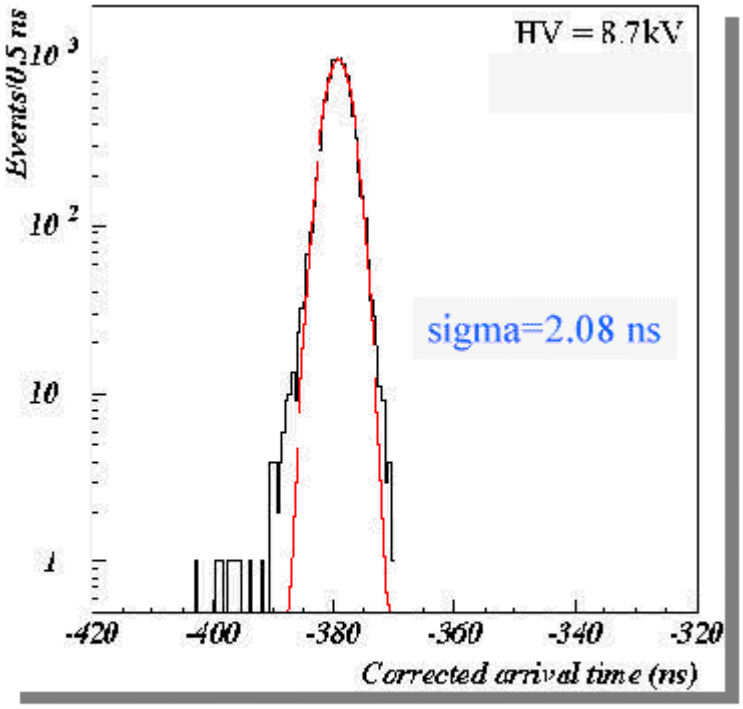

Correction for different signal propagation time along the read-out strips is taken into account by subtracting the time needed by each signal to reach the front-end board (a signal speed of 0.66 c is assumed).

Sigma improves from ~**3 ns** to ~**2 ns**

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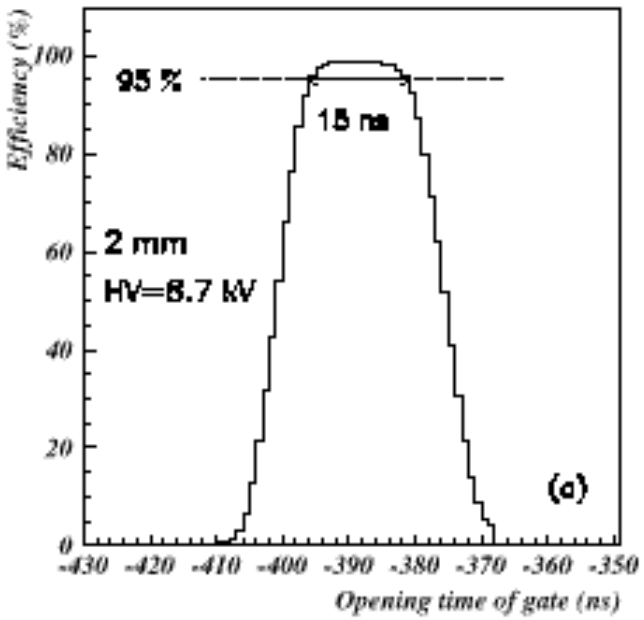
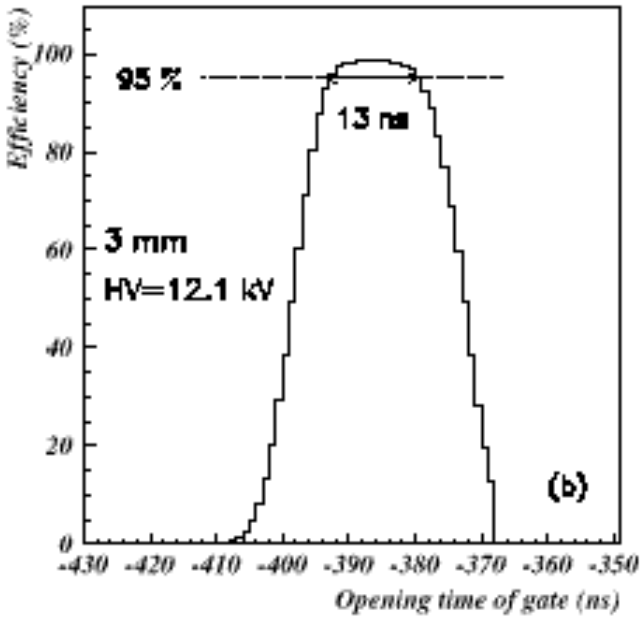
Chamber efficiency as a timing window function





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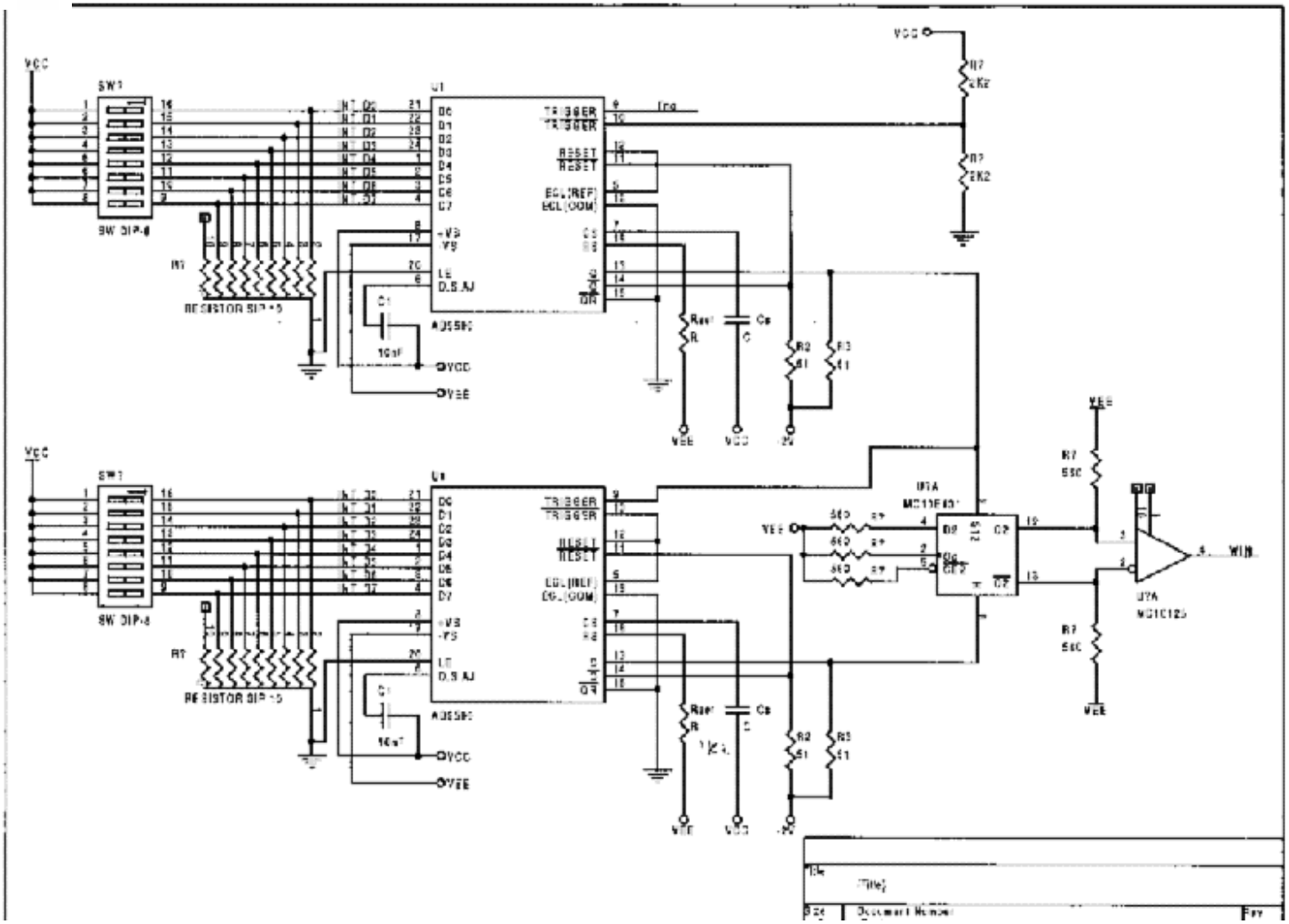
CK & WIN generation test circuit



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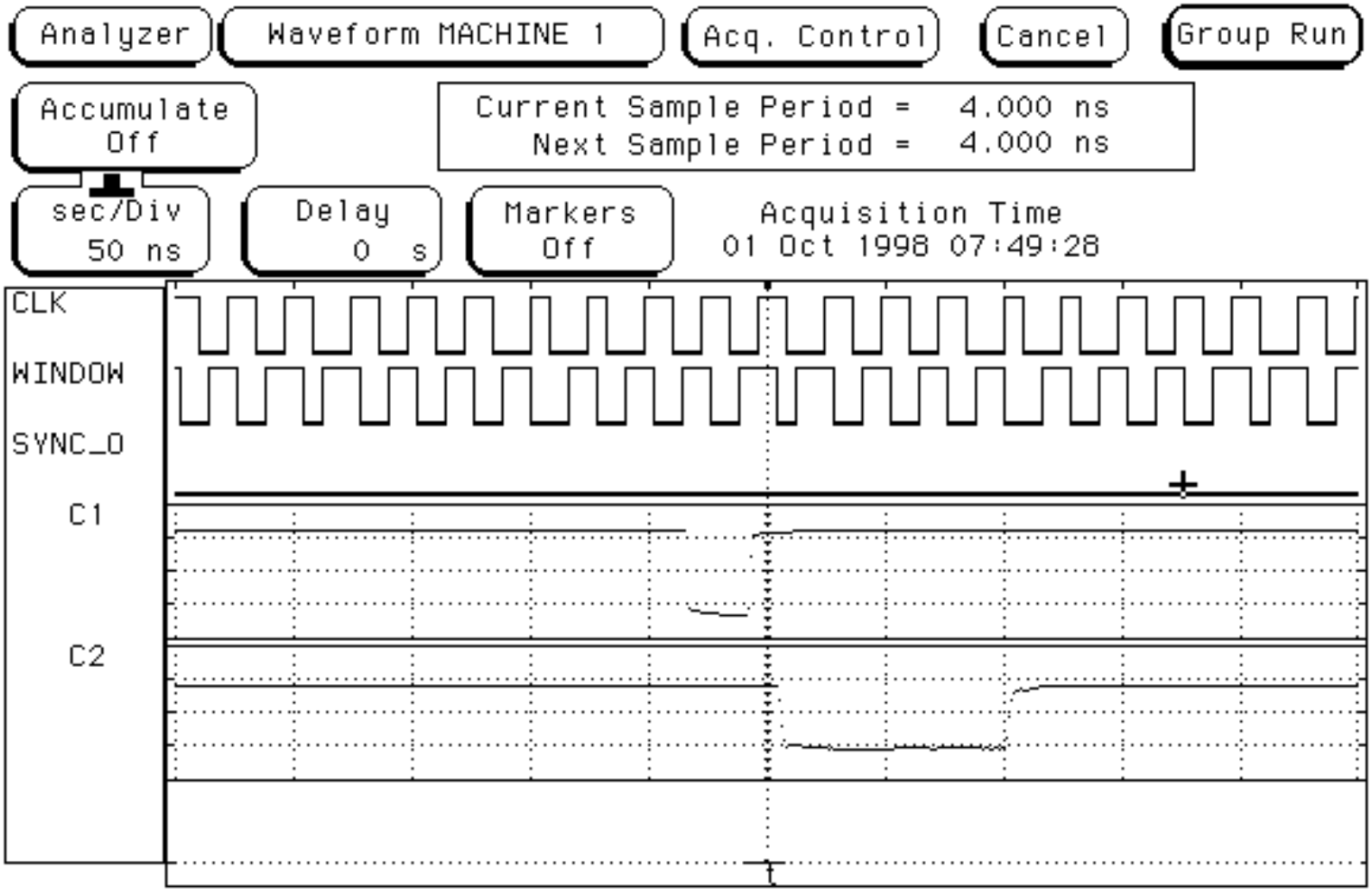
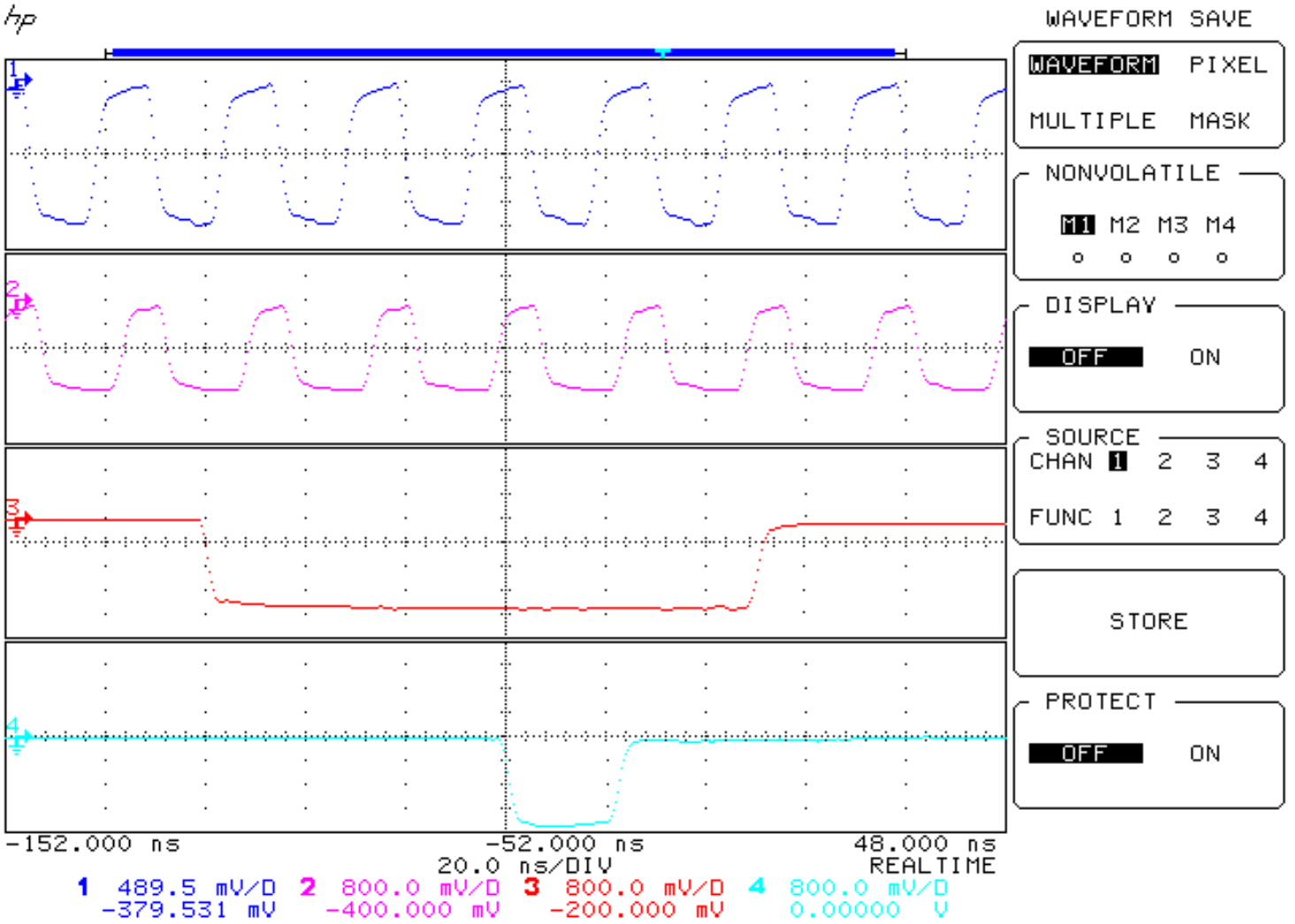
FE board amplifier output



Synchronizer test circuit output

RPC



RPC

NEW FRONT END CHIP FOR RPC DETECTOR OF CMS

- **Charge preamplifier for strip impedance matching (15-30 Ω)**
- **AC - coupling with discriminator for low offset (< 3 fC) and low dead time (< 70 ns)**
- **Zero - crossing discriminator for amplitude - independent timing response (< 3 ns)**
- **One - shot with tunable pulse width**
- **Low - voltage differential line driver (LVDS compatible) with tunable output current**
- **The FE chip will contain 8 channels**
- **developed in 0.8 μ BiCMOS technology by AMS**
- **Foundry run 4 December through CMP**

RPC

Front_End Board Control components

1999 implementation (not final)

- **The Front_End Board will contain 16 RPC channels**
- **Two 10-bit CMOS DAC's with 2.5 V reference voltage & with very low power consumption (3 mW)**
- **Discriminator threshold resolution: 1.2 fC/bit**
- **Low Power CMOS clocked FIFO operating @ 3.3 V, as test pattern generator for the 16 RPC channels**
- **Injected charge for test pattern: 660 fC (discriminating capability: 10 fC < Q_{th} < 300 fC)**
- **Synchronization Unit for the 16 RPC channels controlled by the system Clock (@ 40 MHz) and a Window pulse, with adjustable phase respect to the Clock (feed from external)**
- **OR8 (OR16) functions & histogramming capability integrated in the SU**
- **The various components will be remotely controlled by LB**
- **LVDS output driver**