RPC Muon Trigger Detector Control

Ignacy Kudla, Radomir Kupczak, Krzysztof Pozniak, Antonio Ranieri

5.8 Power and Control Systems

5.8.4.1 General scheme description

In the Fig. 1 a general scheme of the Front End Control system and the data transmission interface to an optical link is shown. In this figure the FEC is a 6 channels amplifier plus a discriminator, a monostable and a differential line driver placed on an ASIC developed for strip readout and 16 of these devices will be mounted over 4 Front End Boards to readout the 96 channels of one RPC layer as indicated the figure.

The RPC Muon Trigger Detector Control (RPC MTDC) system consists out of two branches :

- the detector oriented (MTDC_DO) - control of the RPC chambers
  - HV control,
  - Gas control,
  - temperature and atmospheric pressure control,
  - Front End Board (FEB) LV control,
  - Link Board (LB) LV control,
  - Front End Board discriminator threshold check;

- the data transfer oriented (MTDC_DTO) - controlling different elements of trigger data path
  - FEC test pulse patterns,
  - FEC test pulse sequences,
  - Front End Board discriminator threshold control,
  - SU (Synchronisation Unit)control,
  - SU histograms readout,
  - LMUX test pattern control,
  - LMUX histograms readout.

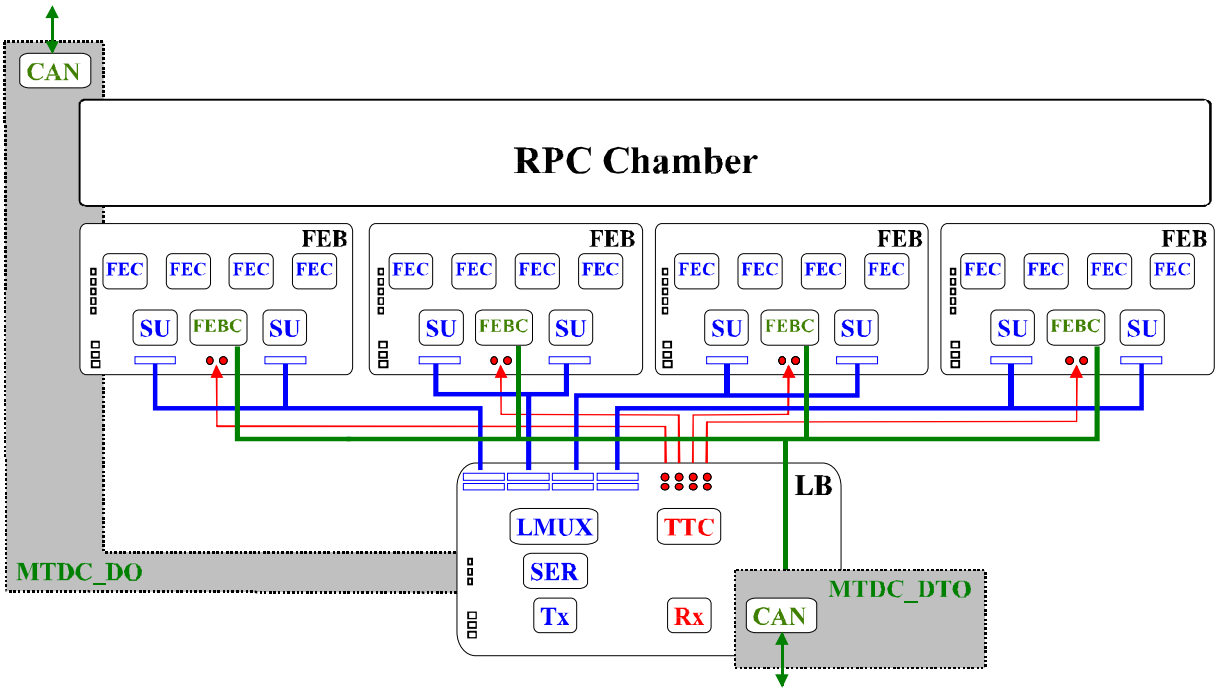

Fig 1.

Two MTDC branches are foreseen to use separate CAN networks.

MTDC_DO network has its own LV power supply, independent from the front end electronics LV supply, because its aim is to control the latter.

MTDC_DTO has a common supply with a LB board, because it is build to control the functioning of trigger data path. One barrel wheel contain 156 RPC chambers (13x12), 7 LB boards (2 LB boards for the reference MB2 RPC layer, 1 LB for others RPC layers).

5.8.4.2 FUNCTIONAL DESCRIPTION

Front End Board (FEB) is a board connected directly to the RPC chamber and contains 24 channels of RPC front end electronics (the physical size of FEB limits the number of channels of Front End electronics). Four FEB's belonging to the same RPC chamber are connected together. FEB's are connected to the LB board, to the LV power supply and to the MTDC_DO branch of MTDC. (see Fig2.)

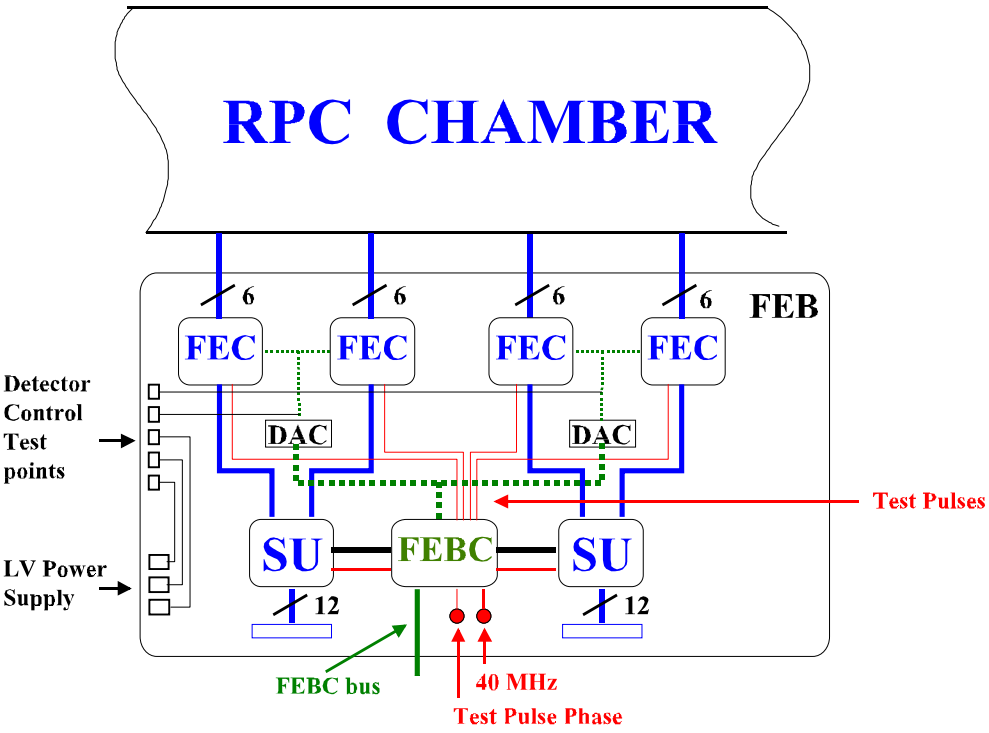

Fig 2.

Front End Board (FEB) accommodates

- 4 Front End Chips (FEC), 6 - channel discriminator and monostable device,
- 2 synchronisation unit (SU) ASIC's,
- Front End Board Controller (FEBC) FPGA.

FEC device contains 6 amplifiers/discriminators/monostables/differential line drivers. Every 3 channels of a FEC device have a common test input (see Fig 3.). Eventually one differential receiver (LVDS like) could be placed on the FEB between the FEC and the SU to convert signal level of the FEC output (300 mV) to a CMOS level signal , in case the SU does not contain itself a differential receiver.

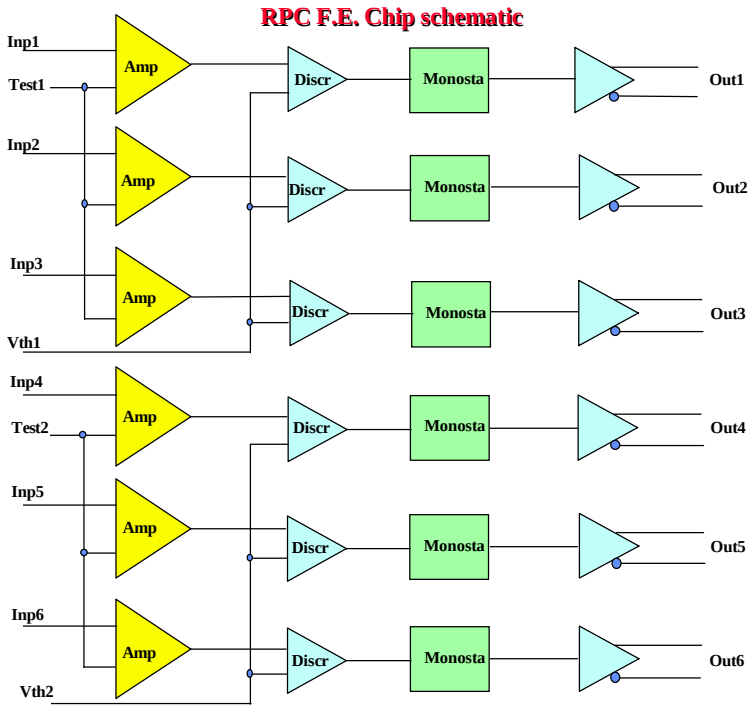

Fig 3.

The Synchronisation unit (SU) stores the FEC's output data if they fit to pre-defined time window within a bunch crossing period and synchronises them with a selected bunch crossing period. SU contains its own histogramming of rates in every data channel. Control of SU's is provided via FEBC bus and FEBC from the LB board.

Front End Board Controller (FEBC) is a device controlling Front End electronics of the RPC chambers.
The objective of FEBC controller is to

- store and distribute the FEC thresholds,
- set the test pattern and test sequence and furnish them in a precise, synchronous way to test input of FEC's,
- set the time window properties for the SU ASIC's,
- read out the SU's test histograms.

Control of the FEBC is provided via FEBC bus from the LB board.
The discriminator thresholds and test bit patterns must be set before enabling the data acquisition. The sequence of tests with one or several test bit patterns can be started with broadcasted test pulse signal after the data acquisition has been enabled.

Link Board (LB) is located close to the RPC and FEB boards. The LB board is supplying the LHC clock, broadcasted test pulses and FEBC bus to the FEB boards. LB board is connected to TTC clock distribution system, to the RPC Trigger Crates (via optical link) and to the MTDC_DTO network. The LB contains the TTC Receiver ASIC (TTCRx), Link Multiplexer (LMUX), LB Controller (LBC) FPGA (and FEBC bus driver) and CAN of MTDC_DTO network. (see Fig 4.)

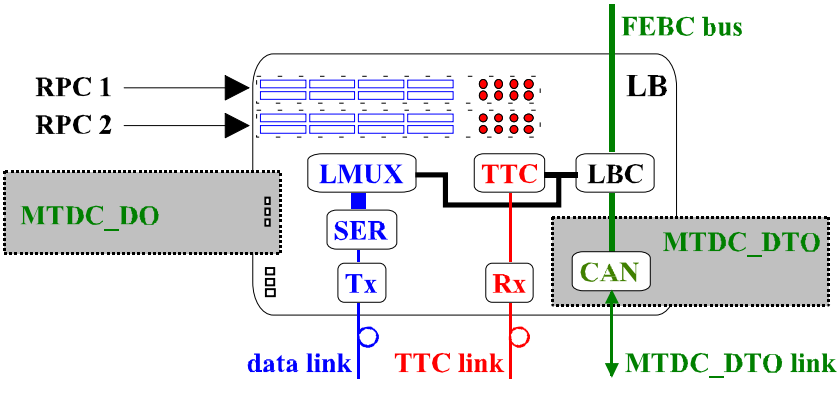

Fig 4.

TTCRx is a part of a timing distribution chain. It furnishes a low jitter clock and test pulse signal for the FE electronics. The timing distribution chain has its own data transmission capabilities (but only in the detector direction) and can be used as an additional (redundance) steering input to the LBC.
LMUX ASIC codes synchronized, not zero RPC data into packets to be send via optical link. (see CMS TN **/97). LMUX is equipped with a data quality circuit which can be used to monitor status of incoming data (from the FEB board). In case of very high input rate (which may overload the link) the part of input data can be masked (set to zero). LMUX has a capability to test the subsequent part of electronics via specific test patterns.

One LB board services two layers of RPC and their front end electronics.

Both branches of MTDC are using CAN chips to build the low cost serial networks.

Data to be controlled and monitored on FEB, LB boards:

discriminator threshold (8 bit),
test bit pattern(8bit/FEB),
test sequence (4bit),
RPC status monitor (read out from SU)
time window position (4bit),
time window length (4bit),
control source (2 bit),
*** to switch control of LBC from MTDC-DTO to TTC,
link data status (8bit), these data are read out via MTDC-DTO,
link test data (8bit) to test the link and following electronics
link configuration (4bit) to close the parts of RPC which are overloading the link.
*** could be placed in SU chip or in LMUX

5.8.2 RPC Low voltage system

The topology for low power distribution is to use local low voltage, low drop-out linear regulators at the front-end electronics and to place switching and low noise power supplies 30 meters away where the magnetic field is about 500 Gauss. In particular for one RPC layer consisting of 96 channels considering only the front-end chips, the receivers (LVDS like), the SU and DAC's with PLL's, we foresee a global consumption of 6600 mW.
In the Fig.5 are shown the connections for LV as is foreseen for two RPC layers and for 2 out of 4 boards per layer.

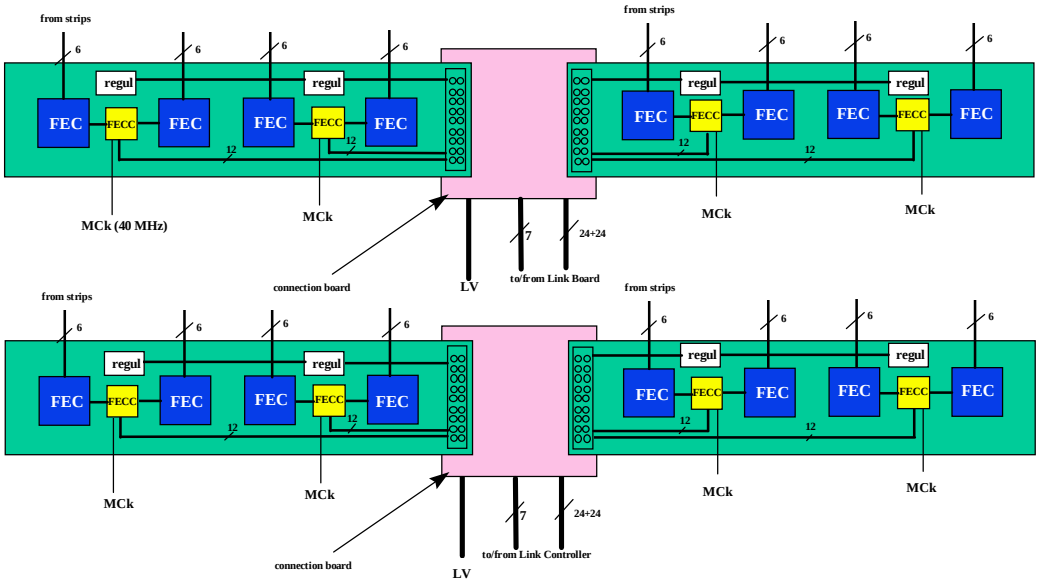

Fig. 5

Each Front-end chip is expected to have two analog power supplies, +3V and -2V and another digital +5V power supply is required for FEBC and SU ASIC. The same +3V power supply should be used for DAC on FEBC. The total current absorption per layer should be of the order of 1.66A. Linear regulators can be connected between the internal power bus and the analog and digital sections of the board separately. By using low drop out devices it is possible to keep the power dissipation in the regulator to a minimum. There are commercial devices with 8 Ch/±3V/3A and with 8 Ch/±12V/1.5A with current protection programmable per

channel having a current resolution of 10mA and a programmable voltage rump-up and rump-down, with a maximum ripple peak to peak at full load of < 5mA, which are appropriate for this application (CAEN SYS 527 system).
One LV cable should be connected to 1/8 of such a type of power supply module. Fuses rated at I > 2 A are necessary at each distribution point of the bus to protect the connector and input traces of each board.
The individual LV lines from any LV channels are designed to avoid large voltage drop across them, which means the cross-section is over-designed for such a current. Under any plausible fault condition, the maximum current that the power supply delivers is lower than the rated current capability of the cables. The voltage drop estimated for these conductors is about 0.8V.

5.8.2 RPC High Voltage system

The High Voltage system should be capable to deliver the appropriate HV values at the current limit set at which the RPC will be operated. A single RPC layer should be operated at about 13 KV with a current limit set to at most 10μA. The use of a system like the CAEN SY127 is envisaged with the possibility, through some no magnetic field sensitive relay to interrupt the supply to a particular noisy chamber. The distribution system should consist of an HV distribution bus with the possibility to switch off under particular current absorption condition exceeding the current set limit, a particular noisy chamber. The scheme to be adopted should be like that one shown in Fig.6.

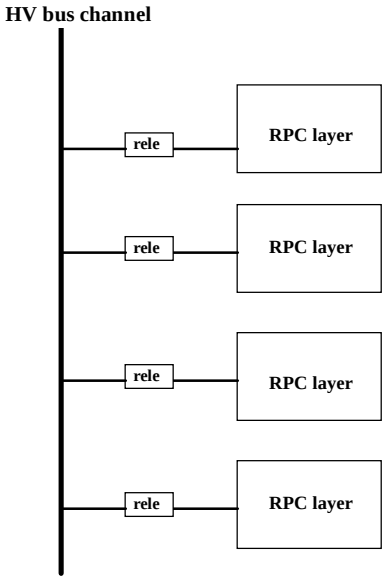

Fig. 6

A number of 20 channels will be allocated per system crate with any channel powering 50 RPC's (we remember that our RPC are equipped as double gaps and therefore two HV channels are required for each RPC).
Any HV module distribution will work with a full scale voltage of 15KV, a voltage resolution of 4 V, a full scale current of 1mA and with a maximum ripple voltage peak to peak < 800mV. The main crate for HV consists of one Std. 19" Euro Crate that houses a Control Unit at the front end, and HV plug-in channels at the rear. The entire system features a software with a friendly user interface, together with over-voltage and over-current protections. The HV system can be locally monitored and controlled via on-board alpha-numeric keypad and display. Remote control is possible via RS-232-C port having the possibility to connect the system control boards of all system crates like a network. Over-current protection is included to protect the system. A fast voltage trip function triggered by a sudden increase in current shut down the supply opening the local switch connected to the related RPC layer and discharge the cable.

5.8.3 Cooling

No particular requirements are foreseen for front-end cooling because the power consumption on the front-end is very limited. The electronics should be encapsulated in boxes mounted directly on the chamber but an air flow circulation in aspiration is required. Some smoke sniffer will be mounted inside the front-end boxes and in case of some smoke presence due to some short-circuit on the front-end boards a forced nitrogen circulation should be provided.