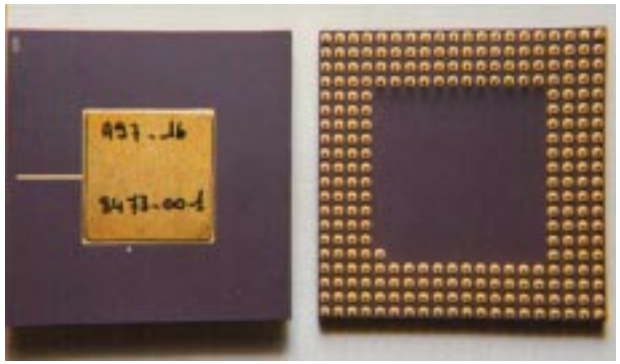
SORTER ASIC for the CMS Muon Trigger

Digital ASIC designed in 0.8μ BiCMOS technology by AMS for the Muon Trigger system in CMS.



The SORTER chip selects the highest 4 objects in absolute value, in an 8 objects group together with their address giving the result in one or two clock cycle.

1. **The chip prototype is implemented using a ceramic package of 257 pins including I/O and power.**
2. **It is developed using 3105 standard cells.**
3. **The die size (core plus I/O pads) is 7.5 x 7.5 mm^2.**
4. **It runs at a frequency of 40 MHz.**
5. **The "Boundary Scan" circuitry is implemented inside the chip in compliance with the JTAG IEEE 1149.1 specifications.**
6. **More than 5000 ASIC will be produced and installed in the CMS Trigger system.**