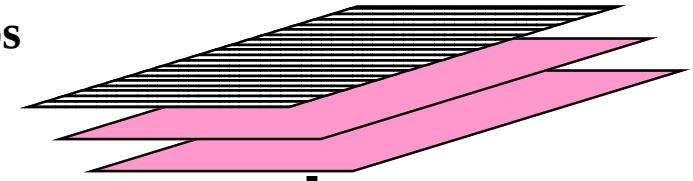
Muon SORTER ASIC Design

- **Sorter chip design: status of the art**
- **Future plans**

TRIDAS, CERN November 3-6, 1997

A. Ranieri INFN Bari

RPC trigger segmentation



~200k strips
Δφ=5/16°
Δη≈0.1

μ recognition
$p_t$measurement
33(39)x12x12=
4752(5616) segments

PAC T (segment processor)
Δφ=2.5°
Δη≈0.1

on 396(468) boards
Δφ=30°
Δη≈0.1

TRB (sector processor) (2 sort levels)

396(468)x4 output

selection of
4 highest p_t μ
in every ring
33(39) rings

ring processor
Δφ=360°
Δη≈0.1
(4 sort levels)

33(39)x4 output

selection of
4 highest p_t μ
in 11(13)
super ring

RPCs/ring sorter (2 sort level)
Δφ=360°
Δη≈0.35

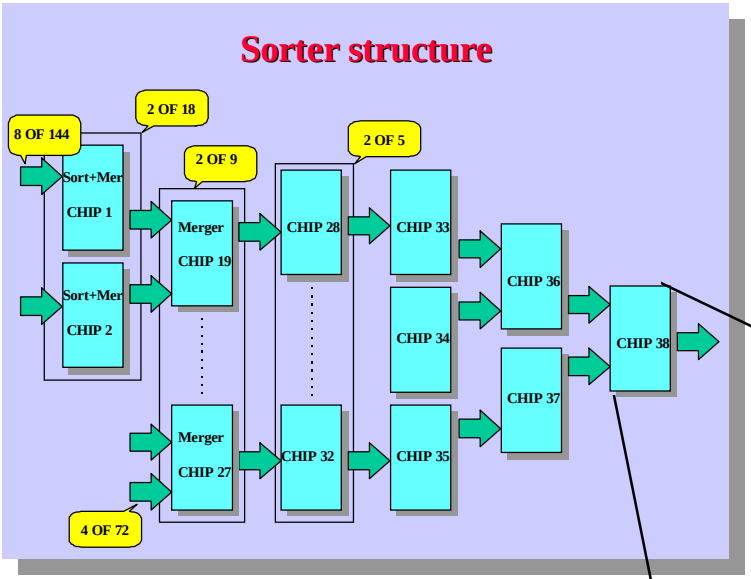
11(13)x4

Global Muon Trigger (4 sort levels)

4 output

MUON SORTING TREE

- **The Sorting Processor chip selects the highest 4 objects in an 8 objects group**
- **We need of a “Sorting Network” to read the whole apparatus**
- **“Tree like structure” subdivided over various levels of processing (8 levels)**
- **The “trigger latency” assigned for sorting RPC data is 8 BX time slot (200ns)**



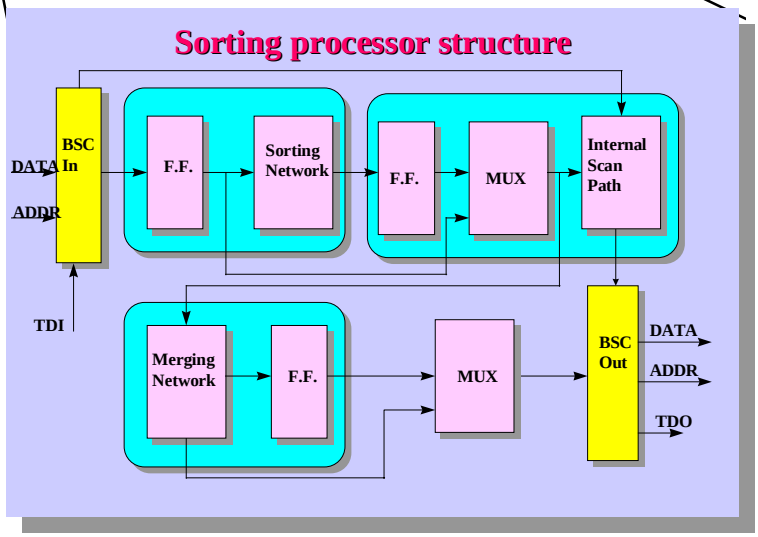
SORTER PROCESSOR CHARACTERISTICS

INPUT	OUTPUT
8 DATA (8 bits)	4 DATA
8 ADDRESSES (8 bits)	4 ADDRESSES

WORD FORMAT

	N. bits
Code	5
Sign	1
Quality	2

1st level: SORTER+MERGER 2 bx
next levels: MERGER 1 bx
last level: MERGER+FF 2 bx



SORTING PROCESSOR CHARACTERISTICS

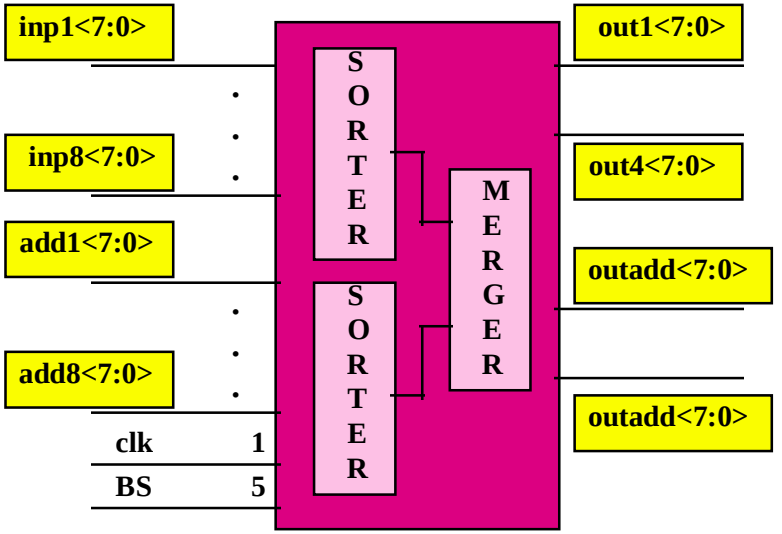
INPUT	OUTPUT
8 DATA (8 bits)	4 DATA
8 ADDRESSES (8 bits)	4 ADDRESSES

WORD FORMAT

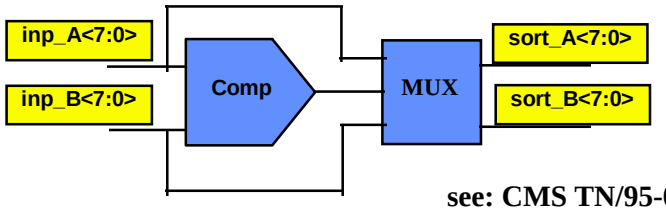
	N. bits
Code	5
Sign	1
Quality	2

1st level: SORTER+MERGER 2 bx
next levels: MERGER 1 bx
last level: MERGER+FF 2 bx

Sorting Processor Chip

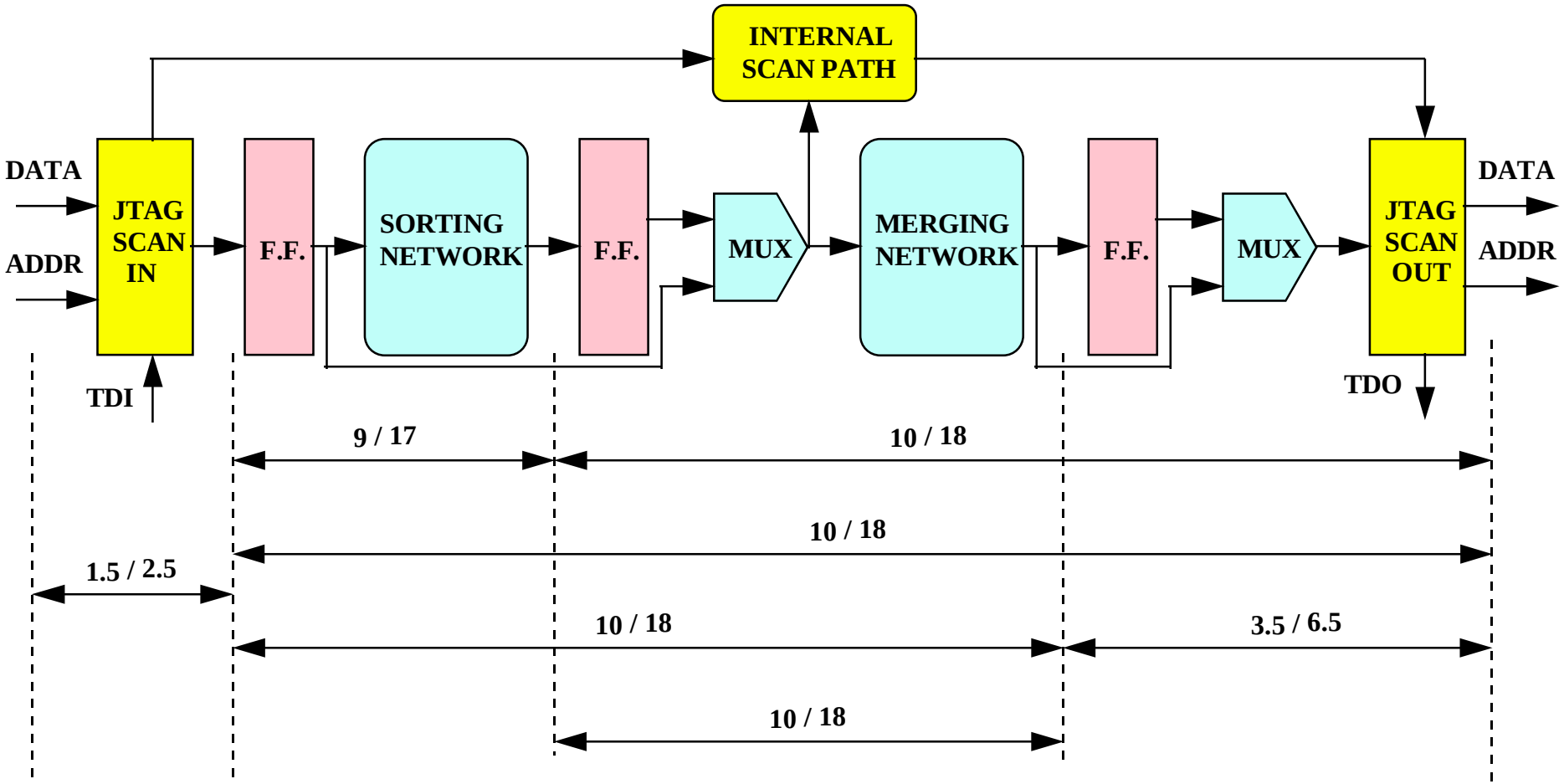


Basic element of Sorting Processor

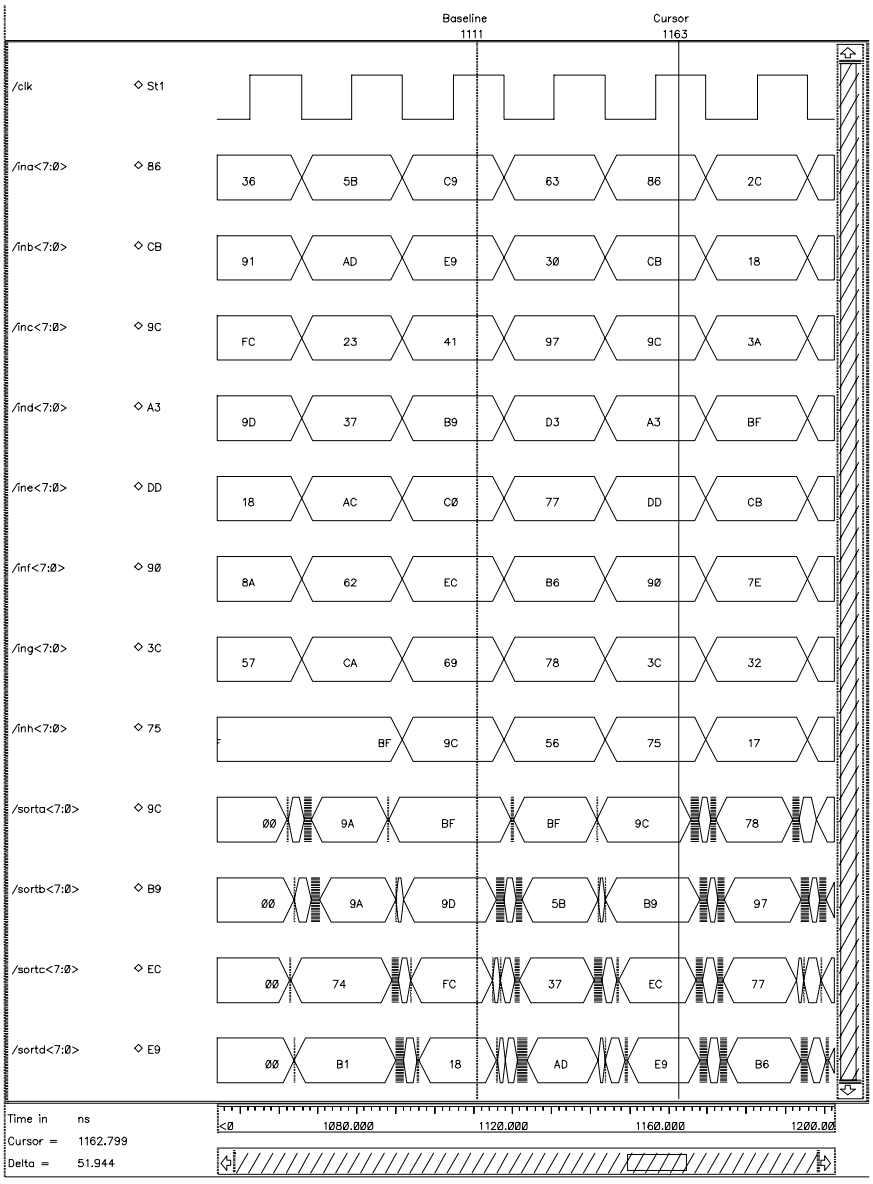


see: CMS TN/95-028

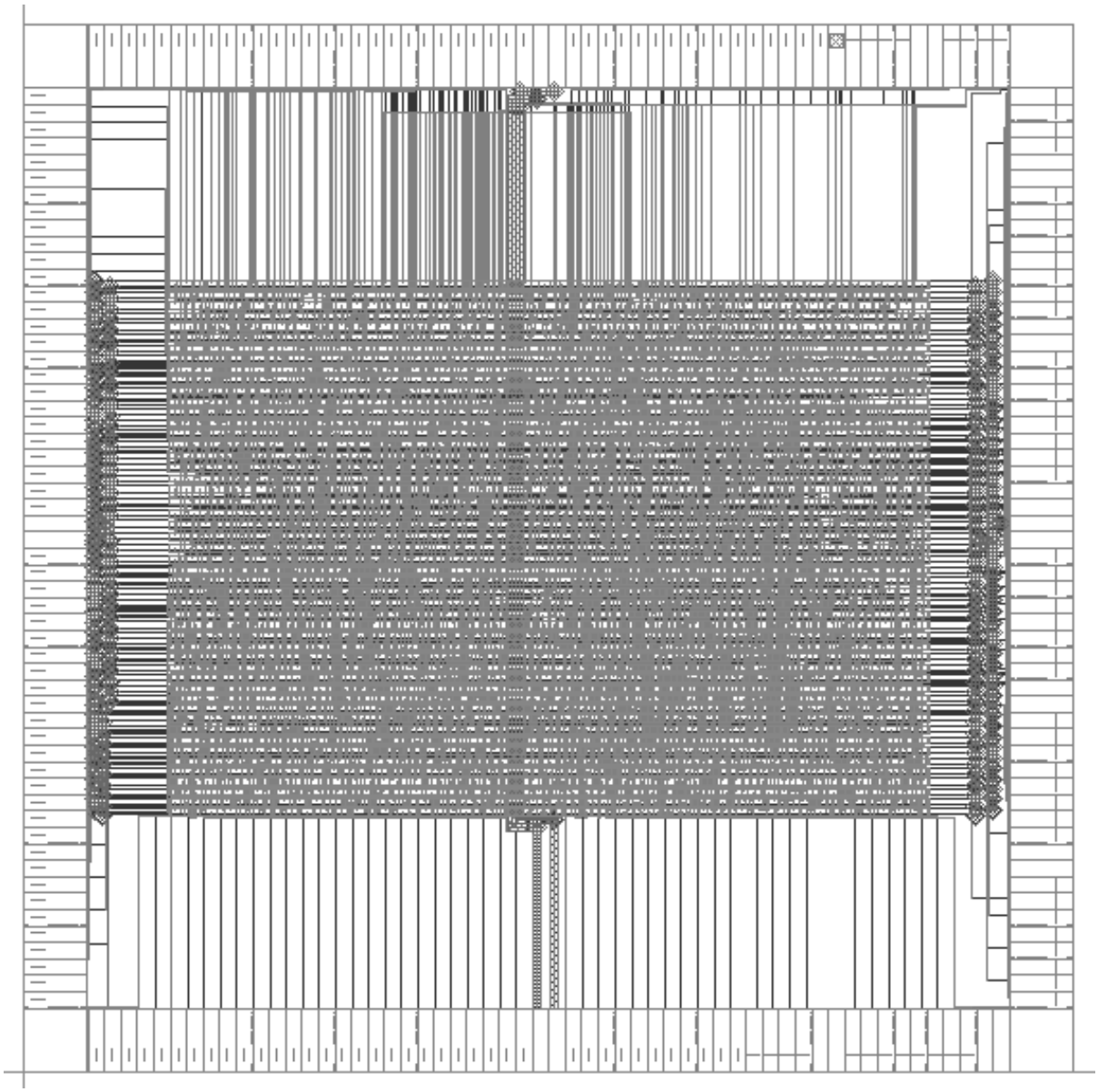
SORTER BLOCK DIAGRAM



ALL DELAYS ARE EXPRESSED IN NS (TYP / MAX)



Typical SORTER + MERGER Verilog simulation



- **Digital semi-custom ASIC using 0.8 μm Bi-CMOS technology by AMS**
- **224 I/O and power pins**
- **JTAG IEEE 1149.1**
- **area: 7.5x7.5 mm^2**
- **40 MHz clock**
- **prototype developing cost: 2600 FF/ mm^2**
- **prototype developing & production by CMS**

RPC Trigger Test Bench

-Designed a Trigger Test Bench made by:

- **Input Board**
- **Synchronization Board**
- **Trigger Board**
- **Read-Out Board**
- **Control & Clock Generator Board**

-installed and tested successfully on an RPC telescope built in BARI (Oct. '96)
-every logic devices was realized with programmable devices (PAC on ALTERA and XILINX for Sorter)
-new trigger electronics for test will be prepared next year mounting the final version of ASICs for PAC & Sorter

Conclusions

- **Prot chip will be delivered next January**
- **Design of a Test Board beginning ‘98**
- **Integration in new TRB 2’nd half ‘98**
- **Order for production during ‘99**