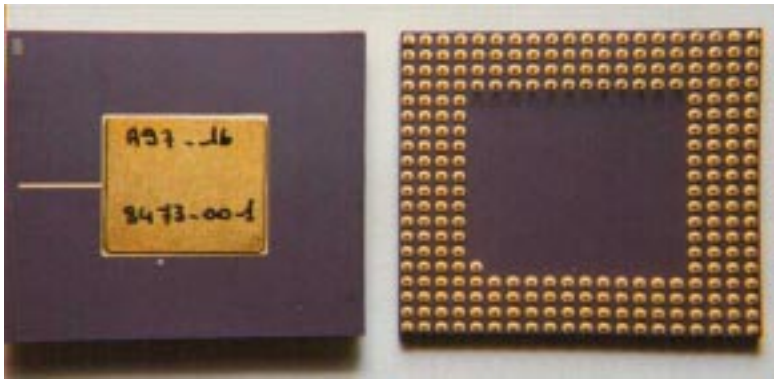
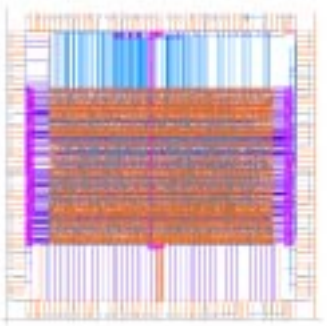
The RPC Muon Sorter Project

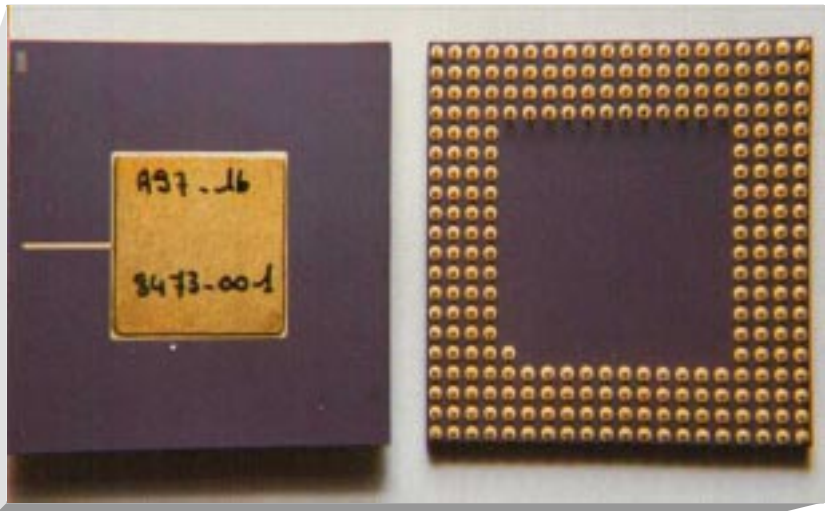
- **Project Status**
- **Prospects**

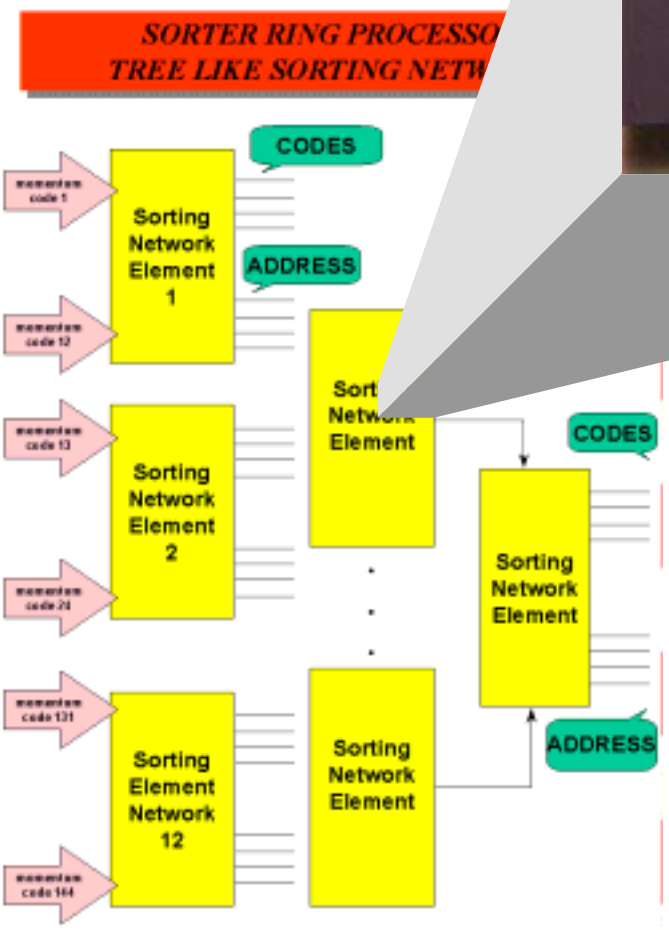


Muon Sorting Tree

- **A Sorting Network Tree like structure selects the highest 4 p_t objects in the whole apparatus**





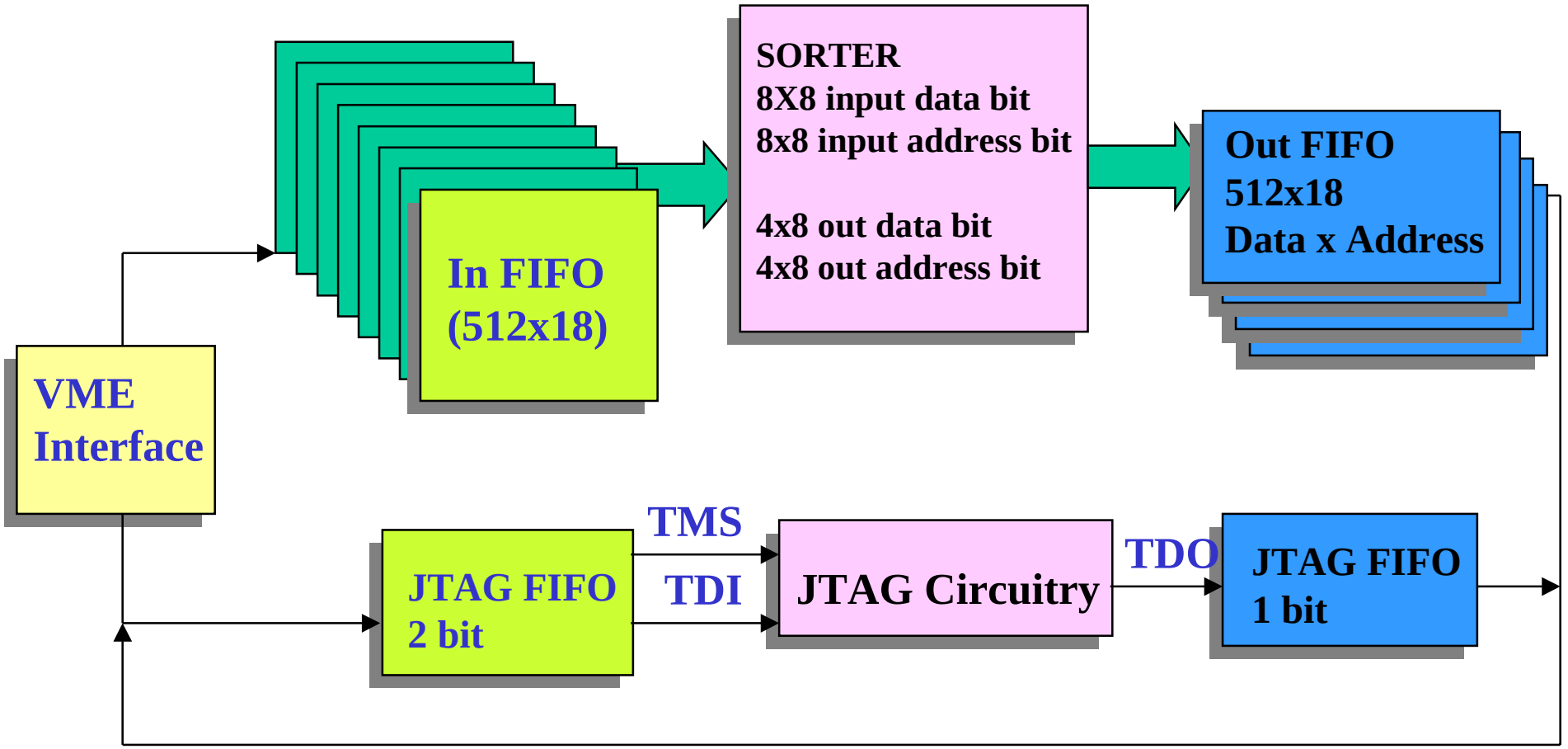


The SORTER Chip

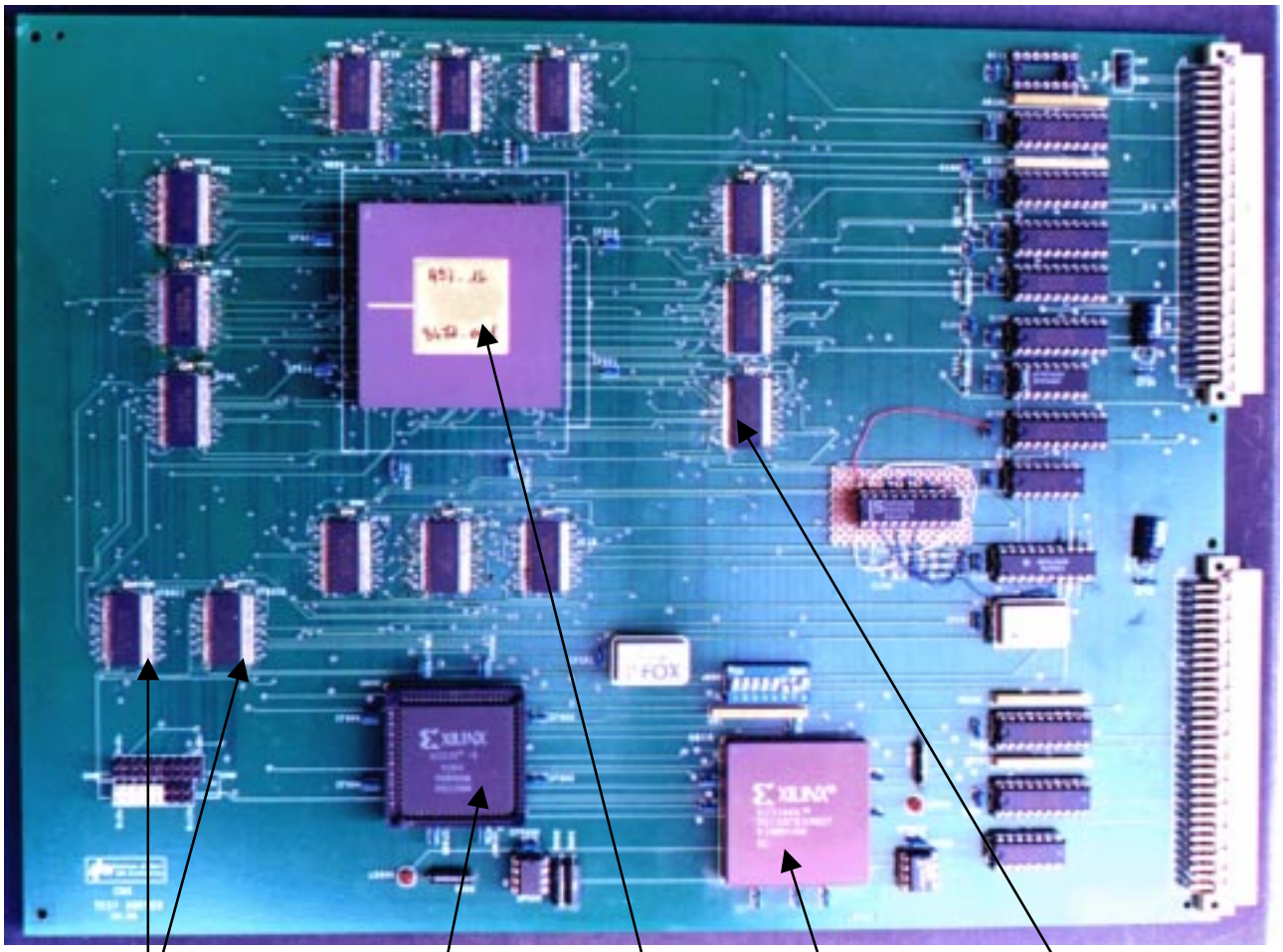
- **Digital semi-custom ASIC using 0.8μ Bi-CMOS technology by AMS**
- **256 I/O and power pins**
- **JTAG IEEE 1149.1**
- **silicon area: 7.5x7.5 mm^2**
- **64 MHz clock**

Input: 8 data (8 bit) Output: 4 data (8 bit)
8 address (8 bit) 4 address (8 bit)
Word Format: 5 code bit, 1 sign bit, 2 quality bit

Sorter Test Board structure



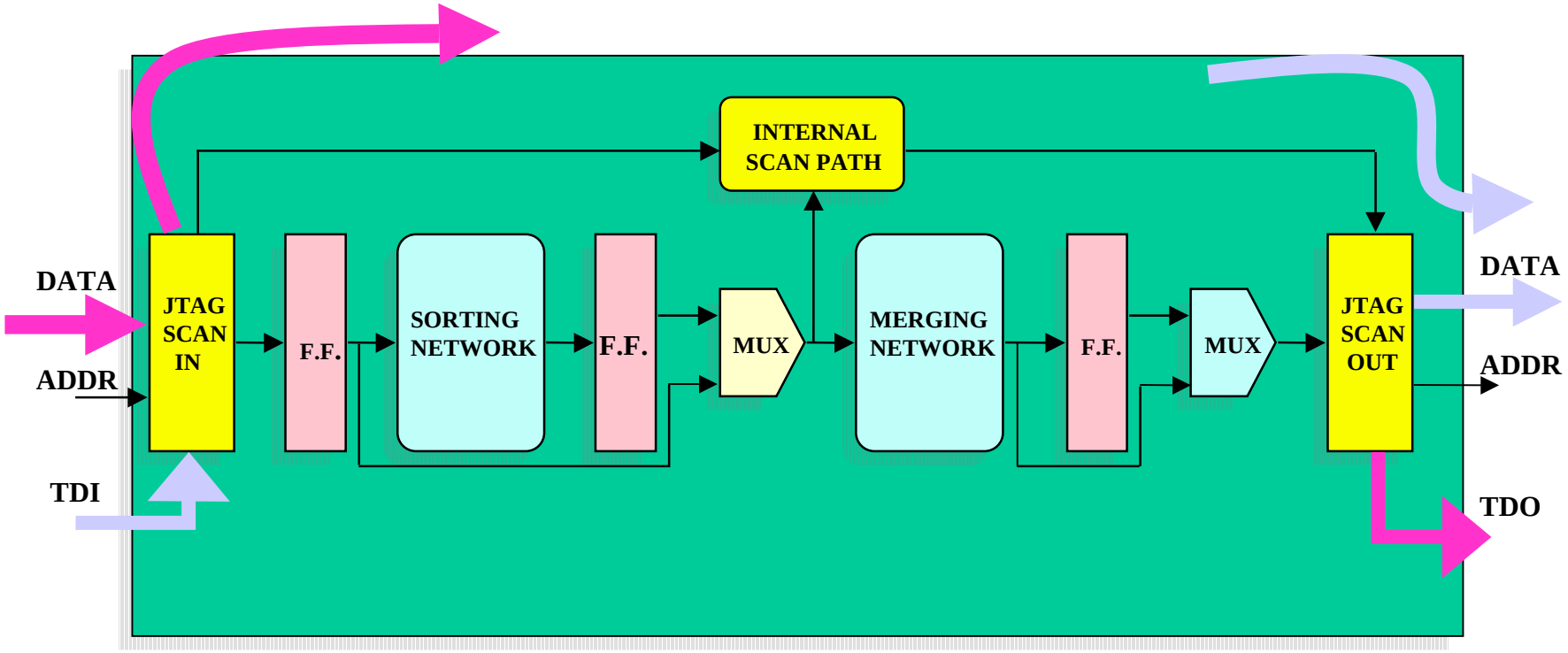
SORTER TEST BOARD



- **Clock @ 66 MHz**
- **Boundary Scan capability**
- **Very simple test procedure**

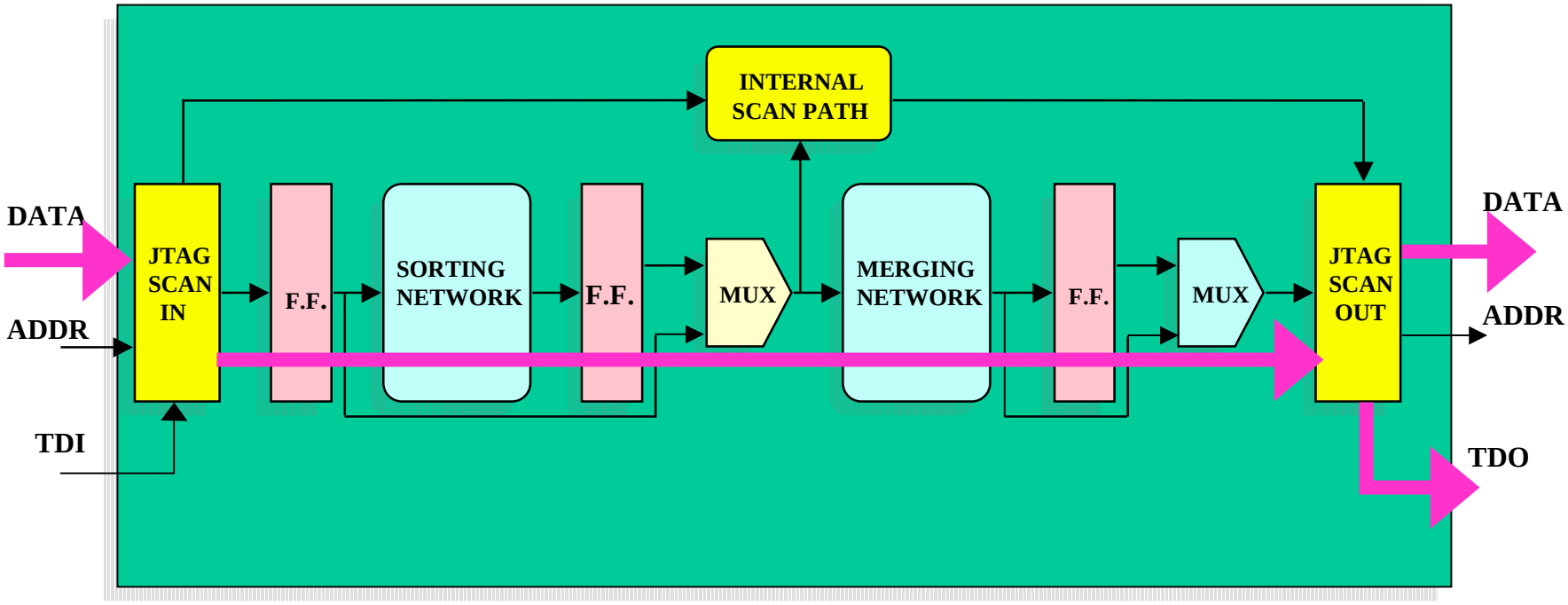
JTAG Flow

Extest case



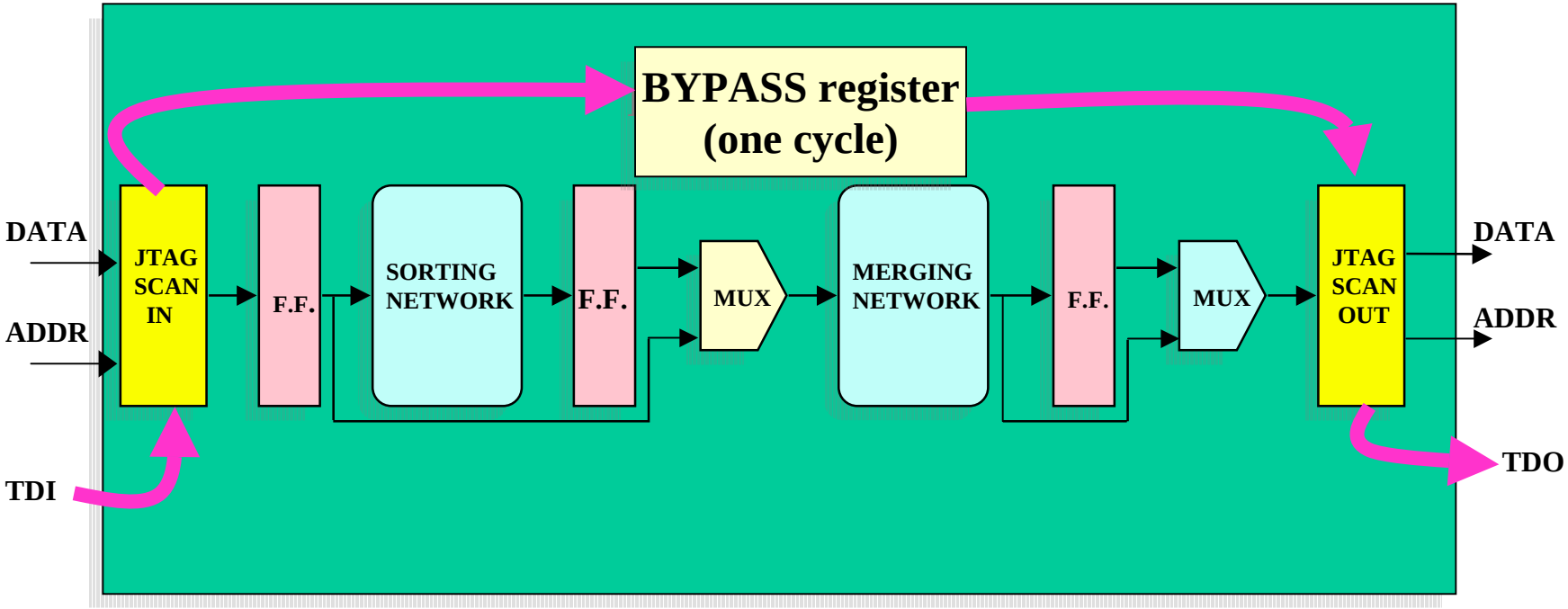
JTAG Flow

Sample case

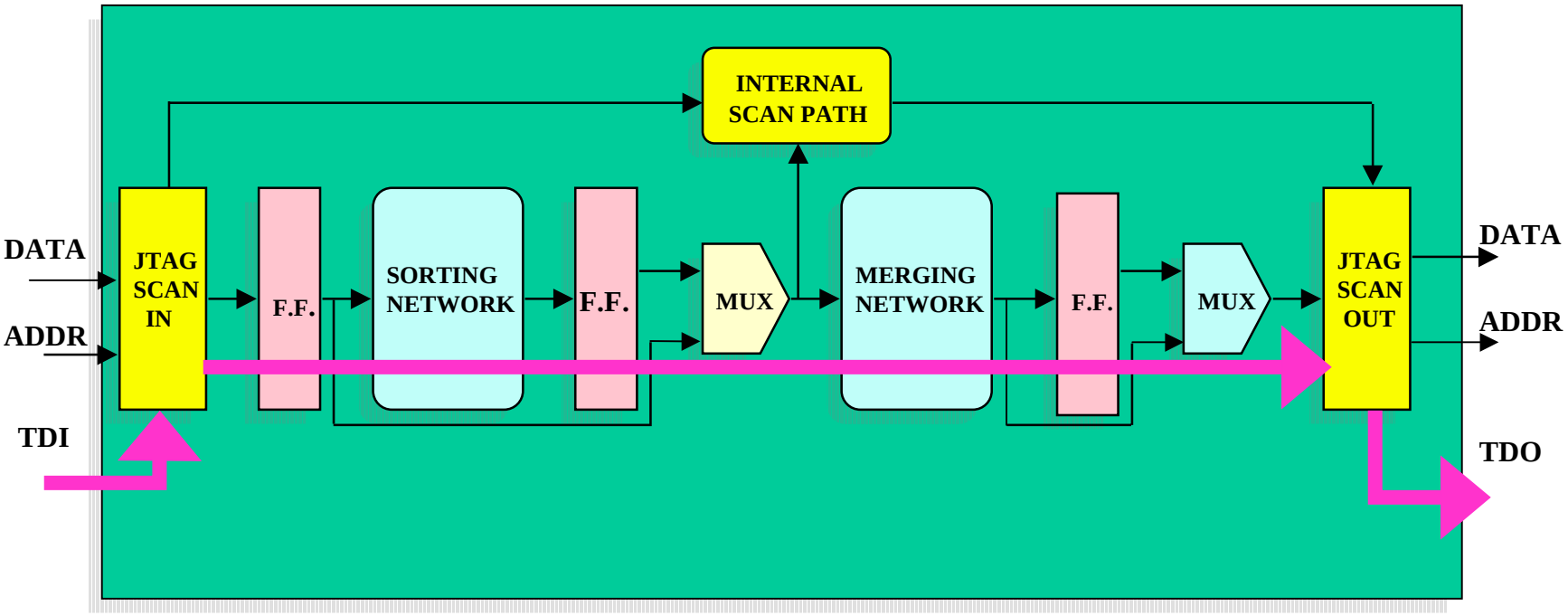


JTAG Flow

Bypass case



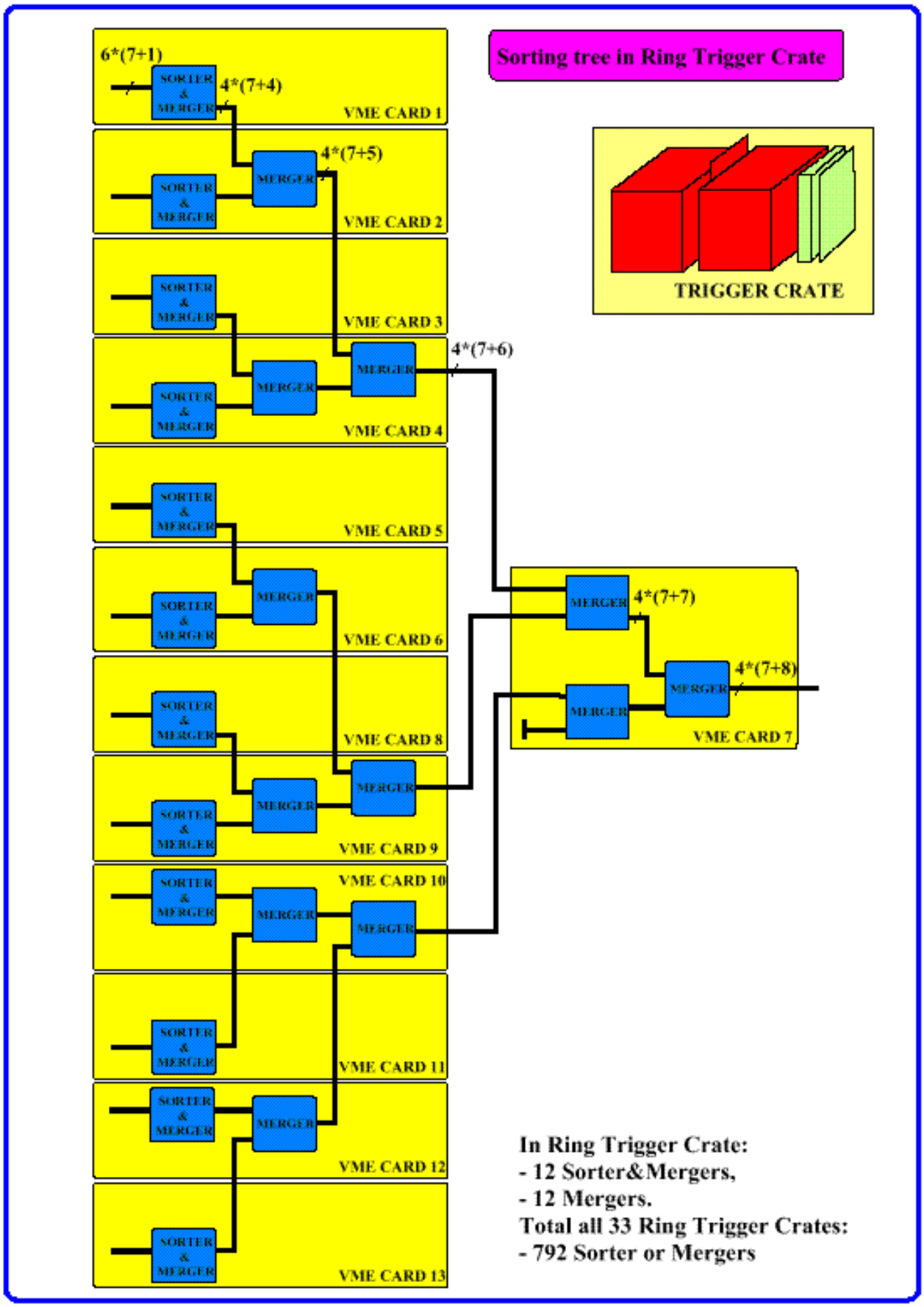
JTAG Flow
INTEST case



SORTER Tests

- **15 packed (256 PGA) chip delivered March '98**
- **Test environment:**
  - **VME Test Board**
  - **JTAG Controller**
  - **Software under OS9 (C language)**
    - **Random Test Pattern generation**
    - **Soft/Hard Test Pattern Check**
- **Test Results:**
  - **2/15 ASICs only no OK**
  - **yield very good, but considering size**

Muon Sorting Tree



Sorter ASIC Results

Merger Output with FF

Cycle0
Input: 0x 4fd 0x5bf2 0x284d 0x3f05 0x1add 0x2db4 0x4c24 0x 8a3
Output: 0x42f7 0x4b74 0x1134 0x454d

Cycle1
Input: 0x637a 0x4053 0x7b71 0x15e9 0x36dd 0x4cd9 0x2ad1 0x51b1
Output: 0x27fd 0x5d37 0x1f15 0x790e

Cycle2
Input: 0x73d7 0x6832 0x6ecf 0x624e 0x7a56 0x75b4 0x3d46 0x3241
Output: 0x1add 0x 4fd 0x2db4 0x5bf2

Cycle3
Input: 0x3f9e 0x385e 0x6888 0x1cc5 0x2112 0x2430 0x3f66 0x5124
Output: 0x36dd 0x637a 0x4cd9 0x4053

Merger output without Out-FF

Cycle0
Input: 0x7974 0x2424 0x11a3 0x43a0 0x4f95 0x3972 0x 26e 0x62a5
Output: 0x 77c 0x3437 0x5c95 0x3e72

Cycle1
Input: 0x61fb 0x24b8 0x3f6e 0x4ecb 0x53bc 0x e59 0x3dae 0x5f87
Output: 0x4f95 0x7974 0x3972 0x 26e

Cycle2
Input: 0x 4b4 0x2970 0x174c 0x7106 0x2d1d 0x4f70 0x7eaf 0x12a3
Output: 0x53bc 0x61fb 0x e59 0x24b8

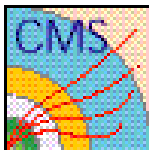
Sorter ASIC Results

Sorter + Merger with Output FF

```
Cycle0
Input:   0x 4250x5bfd 0x284d 0x3fd2 0x1a83 0x2db4 0x4c24 0x
8fd
Output: 0x4bd7 0x4554 0x4234 0x296d

Cycle1
Input:  0x637a 0x4053 0x7b71 0x15e9 0x36d10x4cdd 0x2a91
0x51f9
Output: 0x4bd7 0x4554 0x4234 0x296d

Cycle2
Input:  0x7312 0x686e 0x6ecf 0x62d7 0x7a41 0x7576 0x3d46
0x3294
Output: 0x79dd 0x5c37 0x1f15 0x5d2e

Cycle3
Input:  0x3fc5 0x389e 0x685e 0x1c88 0x2104 0x2466 0x3f30
0x5132
Output: 0x 8fd 0x5bfd 0x2db4 0x3fd2

Cycle4
Input:  0x60bf 0x52e3 0x67e2 0x64b7 0x4d7b 0x2b25 0x5eac
0x1206
Output: 0x4cdd 0x637a 0x51f9 0x4053
```

Sorter ASIC Results

Sorter + Merger without Out-FF



Conclusions

- **Presently Sorter version operating Frequency 66 MHz**
- **Design translation with 0.35/0.25μ technology, is under evaluation**
- **We are quite confident to achieve 100 *MHz* operating condition**
- **Future developing related to DT & CSC final decisions**
- **Integration with Trigger Board**