

# RPC Muon Trigger Detector Control

Ignacy Kudla, Radomir Kupczak, Krzysztof Pozniak, Antonio Ranieri

## A. CMS

### 1. GENERAL

RPC Muon Trigger Detector Control (RPC MTDC) system consists out of two branches :

- detector oriented (MTDC\_DO) - controll of the RPC chambers
  - HV control,
  - Gas control,
  - temperature and atmospheric pressure control,
  - Front End Board (FEB) LV control,
  - Link Board (LB) LV control,
  - Front End Board discriminator threshold check;
- data transfer oriented (MTDC.DTO) - controlling different elements of trigger data path
  - FEC test pulse patterns,
  - FEC test pulse sequences,
  - Front End Board discriminator threshold control,
  - SU control,
  - SU histogram readout,
  - LMUX test pattern control,
  - LMUX histogram readout. ( see Fig 1.)

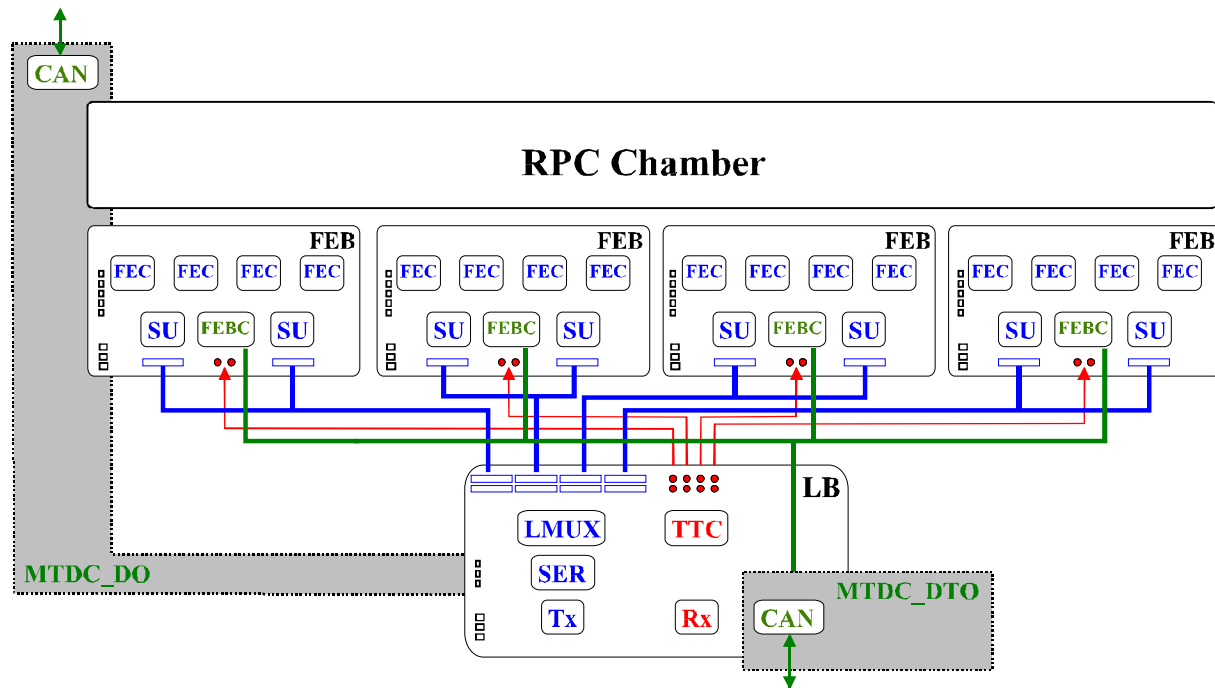


Fig 1.

Two MTDC branches are foreseen to use separate CAN networks.

MTDC\_DO network has its own LV power supply, independent from the front end electronics LV supply, because its aim is to control the latter.

MTDC.DTO has a common supply with a LB board, because it is build to control the functioning of trigger data path. One barrel wheel contain 156 RPC chambers, 7 LB boards (2 LB boards for the reference MB2 RPC layer, 1 LB for others RPC layers).

## 2. FUNCTIONAL DESCRIPTION

**Front End Board (FEB)** is a board connected directly to the RPC chamber and contains 24 channels of RPC front end electronics (the physical size of FEB limits the number of channels of Front End electronics). Four FEB's belonging to the same RPC chamber are connected together. FEB's are connected to the LB board, to the LV power supply and to the MTDC\_DO branch of MTDC. (see Fig2.)

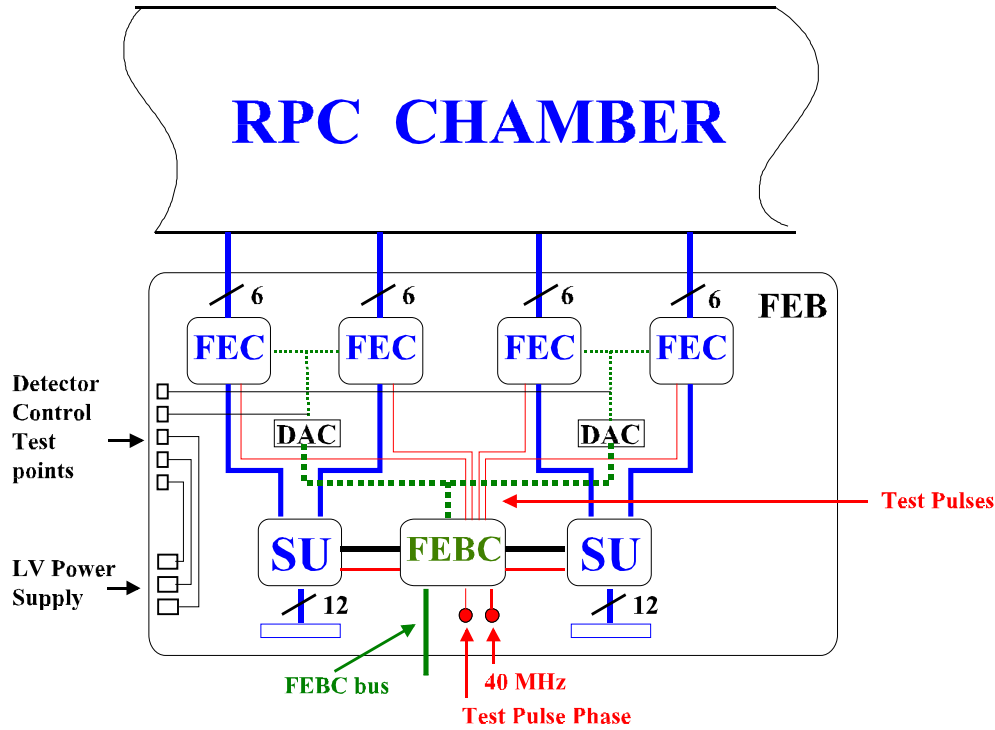


Fig 2.

Front End Board (FEB) accommodates

- 4 Front End Chips (FEC), 6 - channel discriminator and shaper device,
- 2 synchronisation unit (SU) ASIC's,
- Front End Board Controller (FEBC) FPGA.

FEC device contains 6 discriminators/shapers. Every 3 channels of a FEC chip have common test input (see Fig 3.).

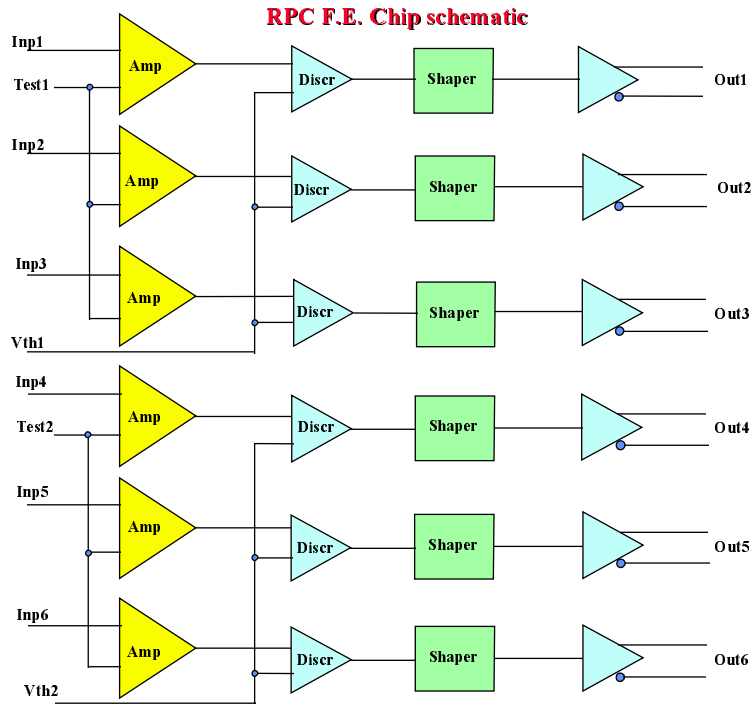


Fig 3.

Synchronisation unit (SU) registers the FEC's output data if they fit to predefined time window within a bunch crossing period and synchronises them with a selected bunch crossing period. SU contains its own histogramming of rates in every data channel. Control of SU's is provided via FEBC bus and FEBC from the LB board.

Front End Board Controller (FEBC) is a device controlling Front End electronics of the RPC chambers. The objective of FEBC controller is to

- store and distribute the FEC thresholds,
- set the test pattern and test sequence and furnish them in a precise, synchronous way to test input of FEC's,
- set the time window properties for the SU ASIC's,
- read out the SU's test histograms.

Control of the FEBC is provided via FEBC bus from the LB board.

The discriminator thresholds and test bit patterns must be set before enabling the data acquisition. The sequence of tests with one or several test bit patterns can be started with broadcasted test pulse signal after the data acquisition has been enabled.

**Link Board (LB)** is located close to the RPC and FEB boards. The LB board is supplying the the LHC clock, broadcasted test pulses and FEBC bus to the FEB boards. LB board is connected to TTC clock distribution system, to the RPC Trigger Crates (via optical link) and to the MTDC.DTO network. The LB contains the TTC Receiver ASIC (TTCRx), Link Multiplexer (LMUX), LB Controller (LBC) FPGA (and FEBC bus driver) and CAN of MTDC.DTO network. (see Fig 4.)

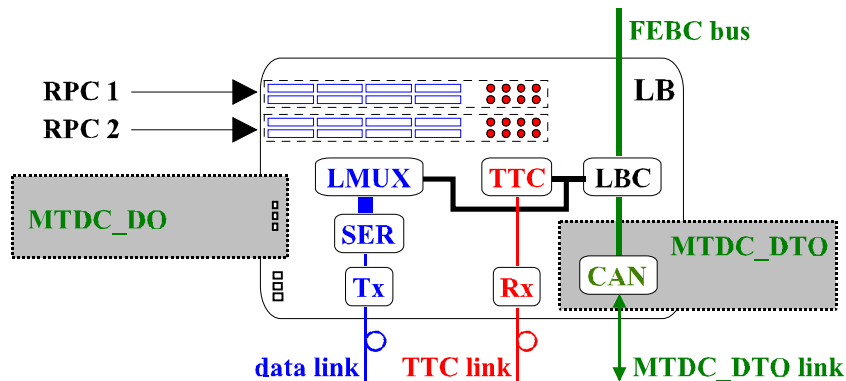


Fig 4.

TTCRx is a part of a timing distribution chain. It furnishes a low jitter clock and test pulse signal for the FE electronics. The timing distribution chain has its own data transmission capabilities (but only in the detector direction) and can be used as an additional (redundance) steering input to the LBC.

LMUX ASIC codes synchronized, not zero RPC data into packets to be send via optical link. (see CMS TN \*\*/97). LMUX is equipped with a data quality circuit which can be used to monitor status of incoming data (from the FEB board). In case of very high input rate (which may overload the link) the part of input data can be masked (set to zero). LMUX has a capability to test the subsequent part of electronics via specific test patterns.

One LB board services two RPC's and their front end electronics.

Both branches of MTDC are using CAN chips to build the low cost serial networks.

\*\*\*

**Data to be controlled and monitored on FEB, LB boards:**

discriminator threshold (6bit),

test bit pattern(8bit/FEB),

test sequence (4bit),

\*\*\* which type of test sequence?

\*\*\* e.g.: two bit vectors in distance of 1bx , 2bx,etc

RPC status monitor (read out from SU)

time window position (4bit),

time window length (4bit),

control source (2 bit),

\*\*\* to switch control of LBC from MTDC-DTO to TTC,

link data status (8bit), these data are read out via MTDC-DTO,

link test data (8bit) to test the link and following electronics

link configuration (4bit) to close the parts of RPC which are overloading the link.

\*\*\* could be placed in SU chip or in LMUX?

\*\*\*

## B. Bari Test Bench Stand

In Bari Test Bench stand only new, fast chambers will be equipped with FEBC's.

In first version TTC clock and test pulse will be clocked up by Test Bench master clock and related to them test pulse. Link connection between Front End electronics and Test Bench will be replaced with direct digital signal connection.

Fig 5. shows Bari RPC Test Bench stand with 2 new RPC chambers.

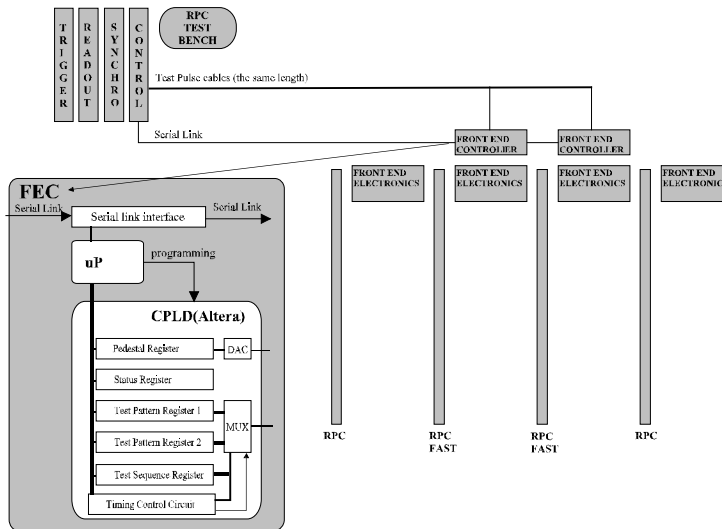


Fig 5.

Bari RPC Test Bench stand Control chain includes two parts :

1. Located on the Test Bench Control board :
  - 1.1. interface to Test Bench clock, supplying test pulse with programmable delay and width;
  - 1.2. serial link daughter card providing connection of CAN chain to the VME;
2. Located on RPC chamber
  - 2.1. serial link daughter card providing connection to the CAN chain,
  - 2.2. uP used to load Altera,
  - 2.3. Altera's FPGA containing the all FEBC's registers,
  - 2.4. DAC's providing the analog voltage sources to the discriminator and shaper,

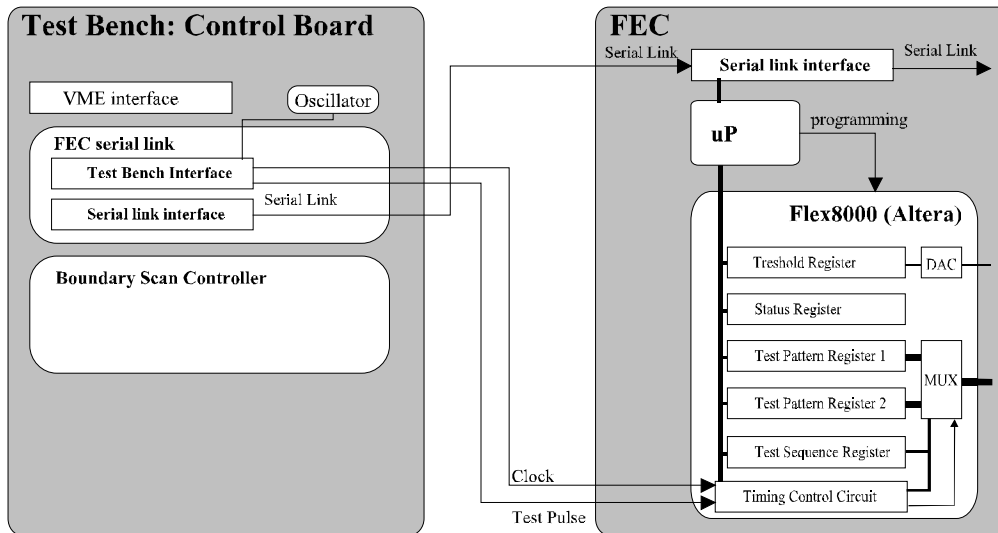


Fig 6.