NEW FRONT-END CHIP FOR RPC DETECTOR OF CMS

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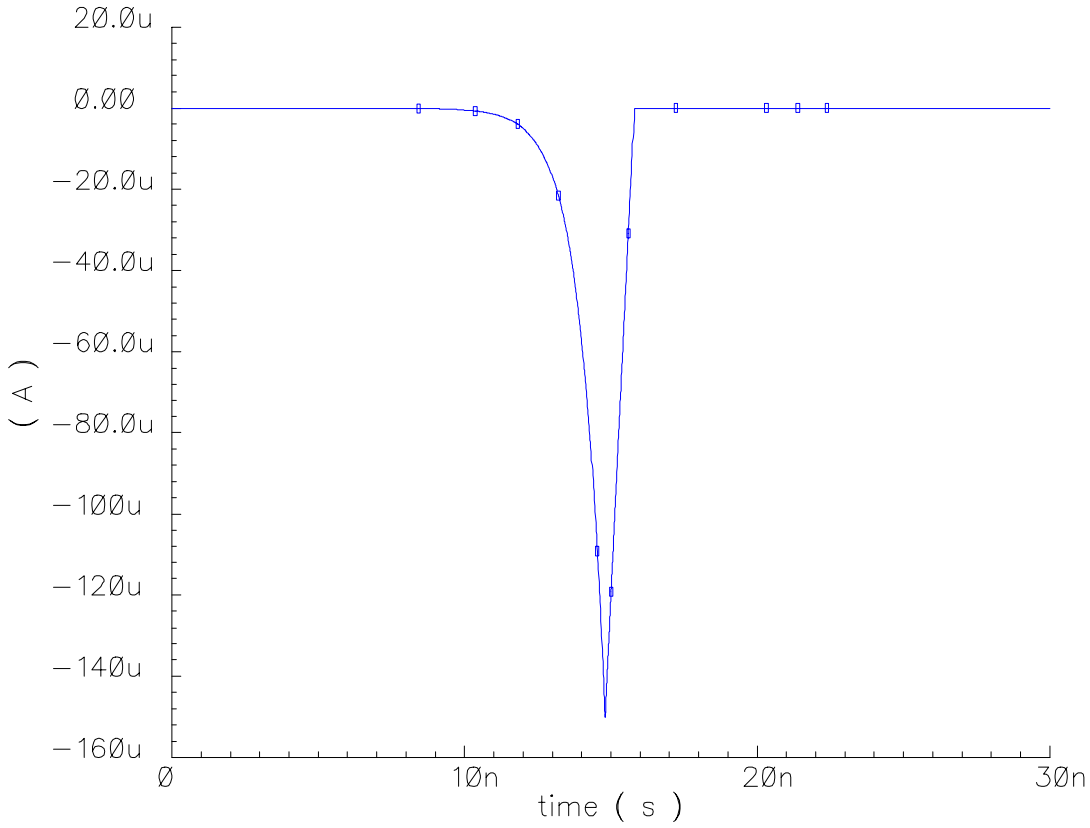
For the RPC CMS BARI-PAVIA Collaboration

Shape of the signal: $I(t) = I_0 \exp(t/\tau)$ $(0 \leq t \leq 15$ ns)

$\tau = 1/\eta v$ (~ 0.8 ns, at detector working point)



Strip line 1.3 m long and 2 - 4 cm wide:

$15\ \Omega \leq R_0 \leq 40\ \Omega$

$160\ \text{pF} \leq C_{strip} \leq 350\ \text{pF}$

Propagation delay ~ 5.5 ns/m

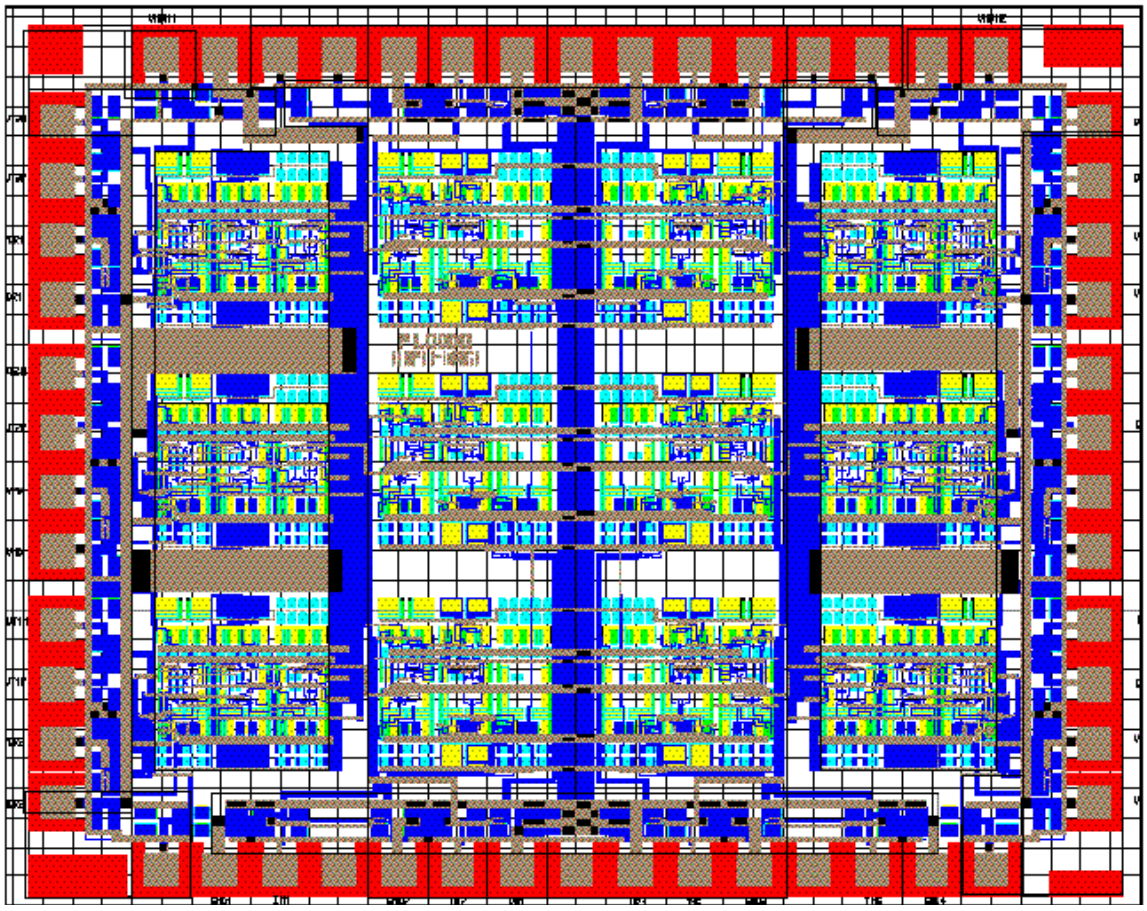
- **Input dynamic range**: $20\ \text{fC} \leq Q_{in} \leq 20\ \text{pC}$

Expected rate: < 400 KHz

FIRST PROTOTYPE

- **TECHNOLOGY: Semi-custom bipolar technology SHPI by MAXIM**

- **6 CHANNELS of Amplifier, Leading edge discriminator, One-shot, differential line driver**



TEST RESULTS OF FIRST PROTOTYPE

- **25 prototypes tested**
- **good agreement with simulations and design parameters of**

1. power consumption (30 mW/chan)
2. charge sensitivity (1.6 mV/fC)
3. noise (~ 2 fC rms)
4. timing performances

- **threshold uniformity unsatisfactory**

expected value ~ 3 fC rms
measured value ~ 6 fC rms

Simulation models do not include mismatch parameters.

- **Used with success at the beam tests (1997, 1998) at CERN**

NEW CIRCUIT

Improvements:

- **Input impedance = 15 Ω**
- **Better threshold uniformity (low offset at discriminator input)**
- **Non-linear amplifier for dynamic compression**
- **Improved timing performances (Zero Crossing Discriminator)**

NEW CIRCUIT

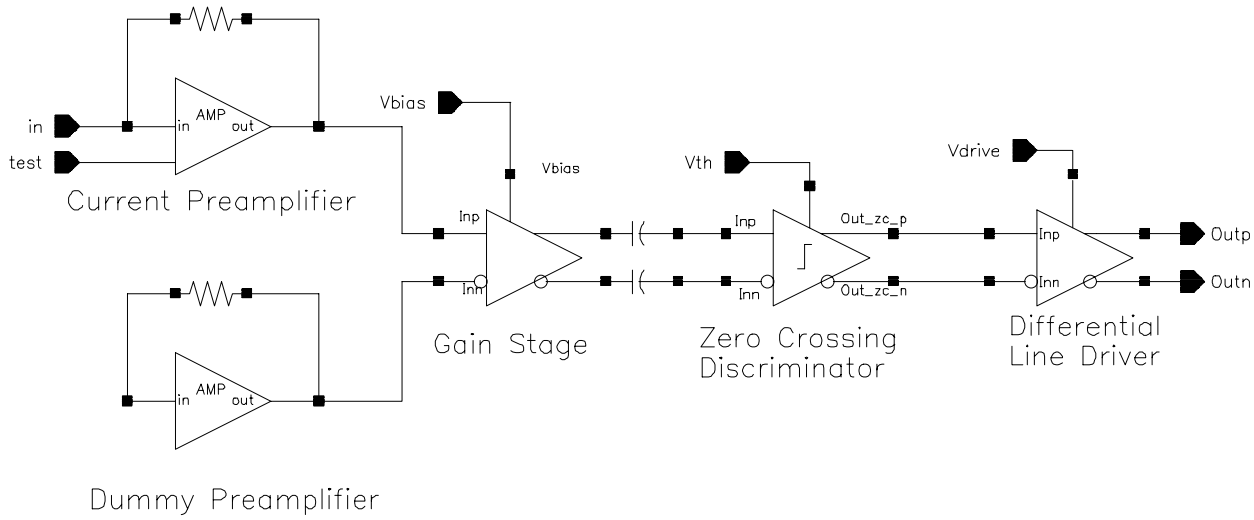
Technology: 0.8 μm BiCMOS of AMS (supported by multiprojects)

8 channels, each one made of:

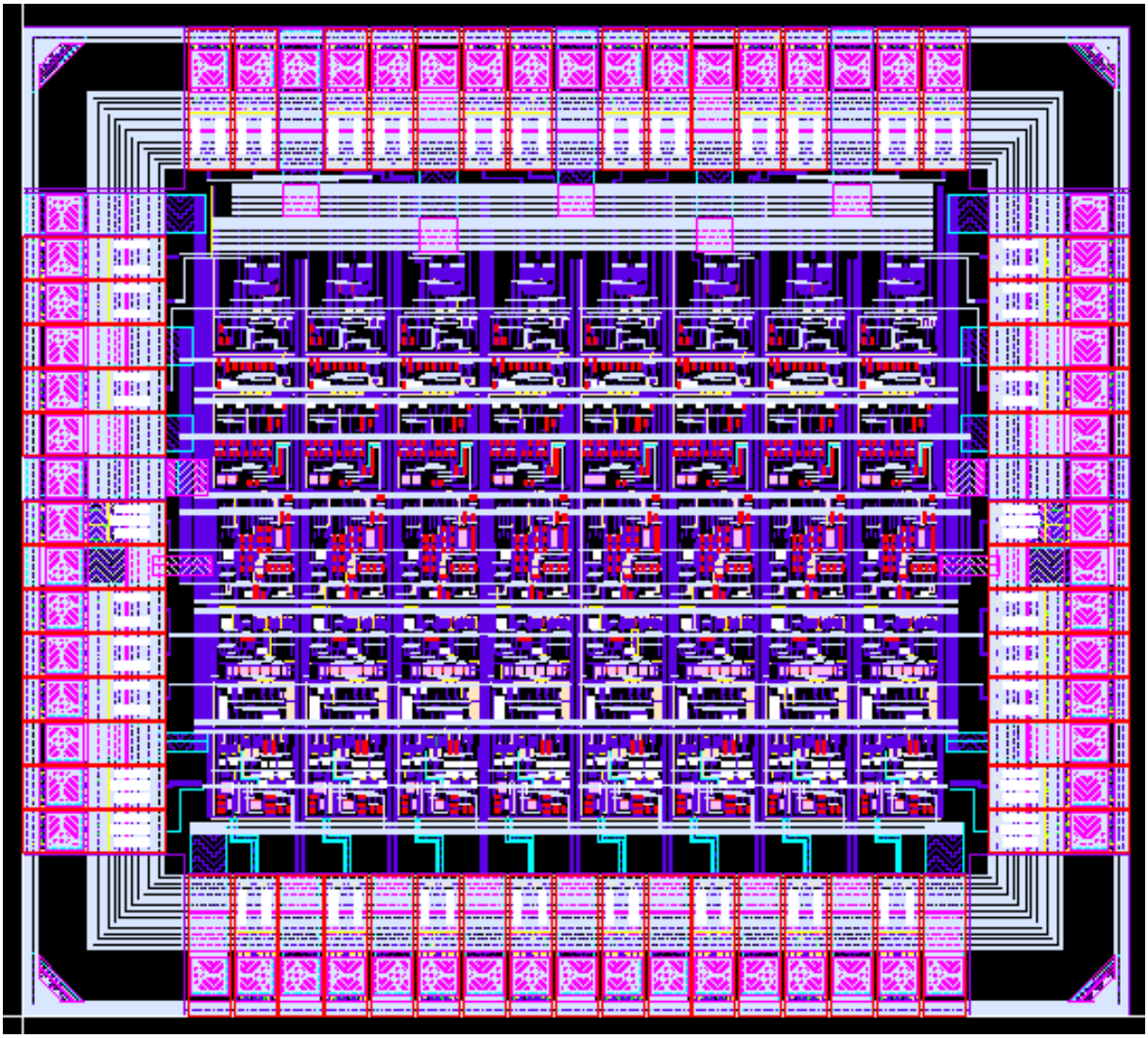
- **amplifier**
- **zero-crossing discriminator**
- **one-shot**
- **differential line driver.**

Power supplies: +5 V; GND

Power consumption: ~ 40 mW/channel



One channel block diagram



Layout of the chip

- **Dimensions: 2.9 mm X 2.6 mm**
- **64 I/O pads**
- **Package: QFP 68**

AMPLIFIER

Must preserve the fast slope of the input signal for fast timing!!!

1. **Current-sensitive preamplifier for strip impedance matching at the signal frequency (~ 100 MHz)**

2. **Gain stage**

- **Power consumption ~ 12 mW**
- **ENC_{TOT} (strip connected and terminated) < 2 fC**

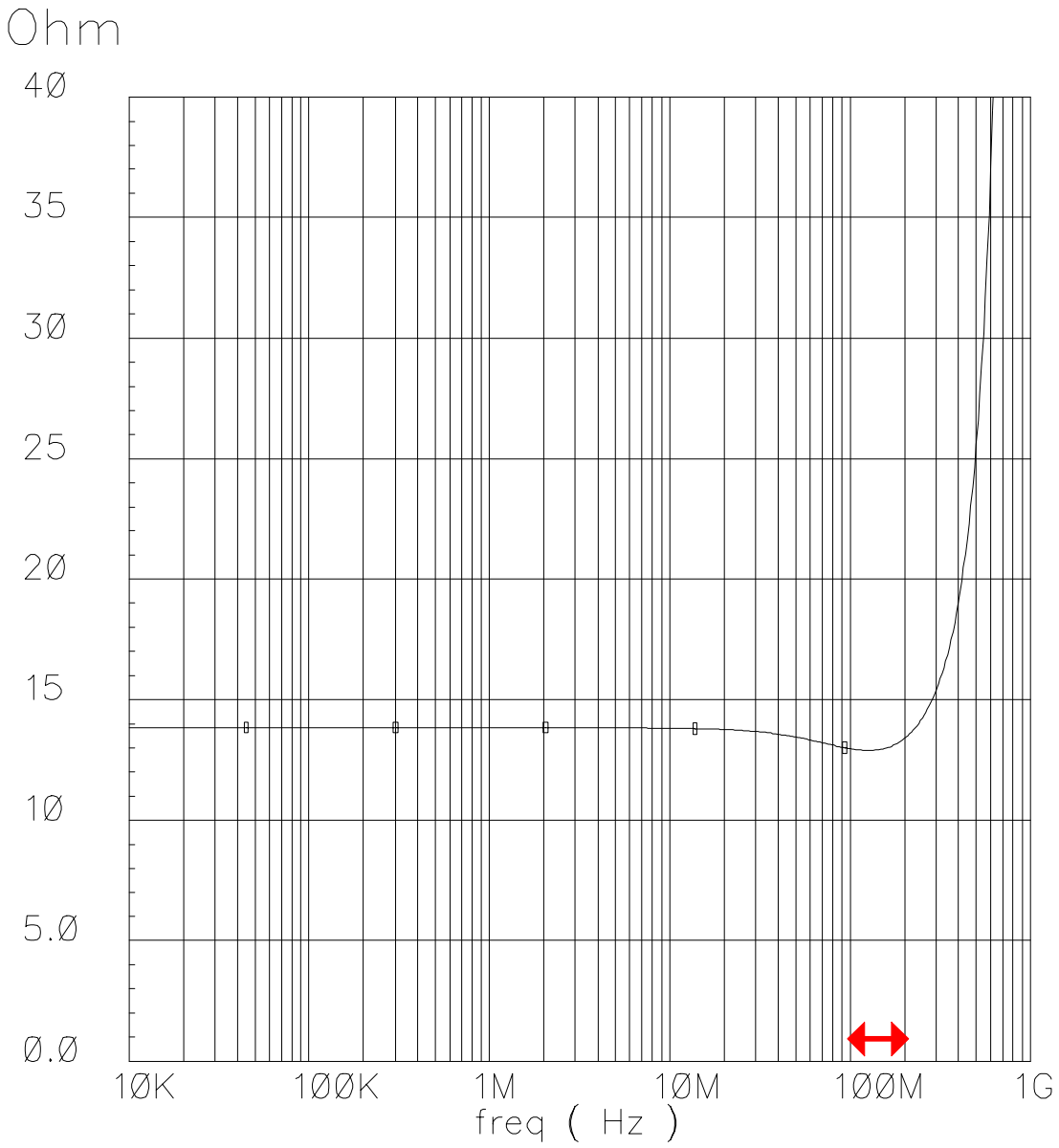
⇓

Threshold: 10 fC

PREAMPLIFIER

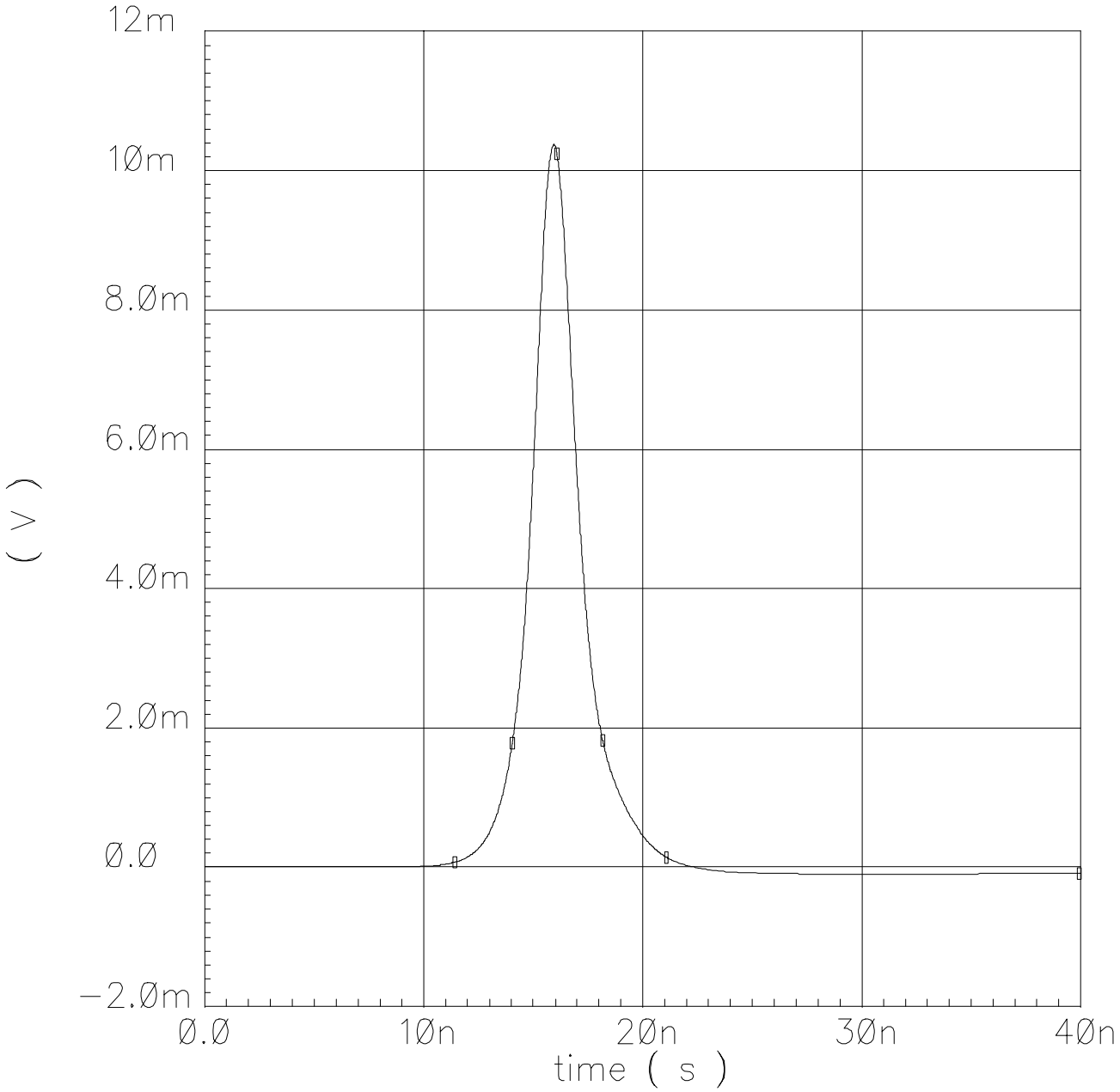
Common emitter transresistance stage

- **Low input impedance: R_{in} ~ 15 Ω**
- **Preserve the shape of input signal**
- **Bandwidth : 116 MHz**



Input impedance vs. frequency

Typical preamplifier response (Qin = 20 fC)



GAIN STAGE

Non linear amplifier for dynamic compression

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Its output is a “peaked pulse” in the dynamic range

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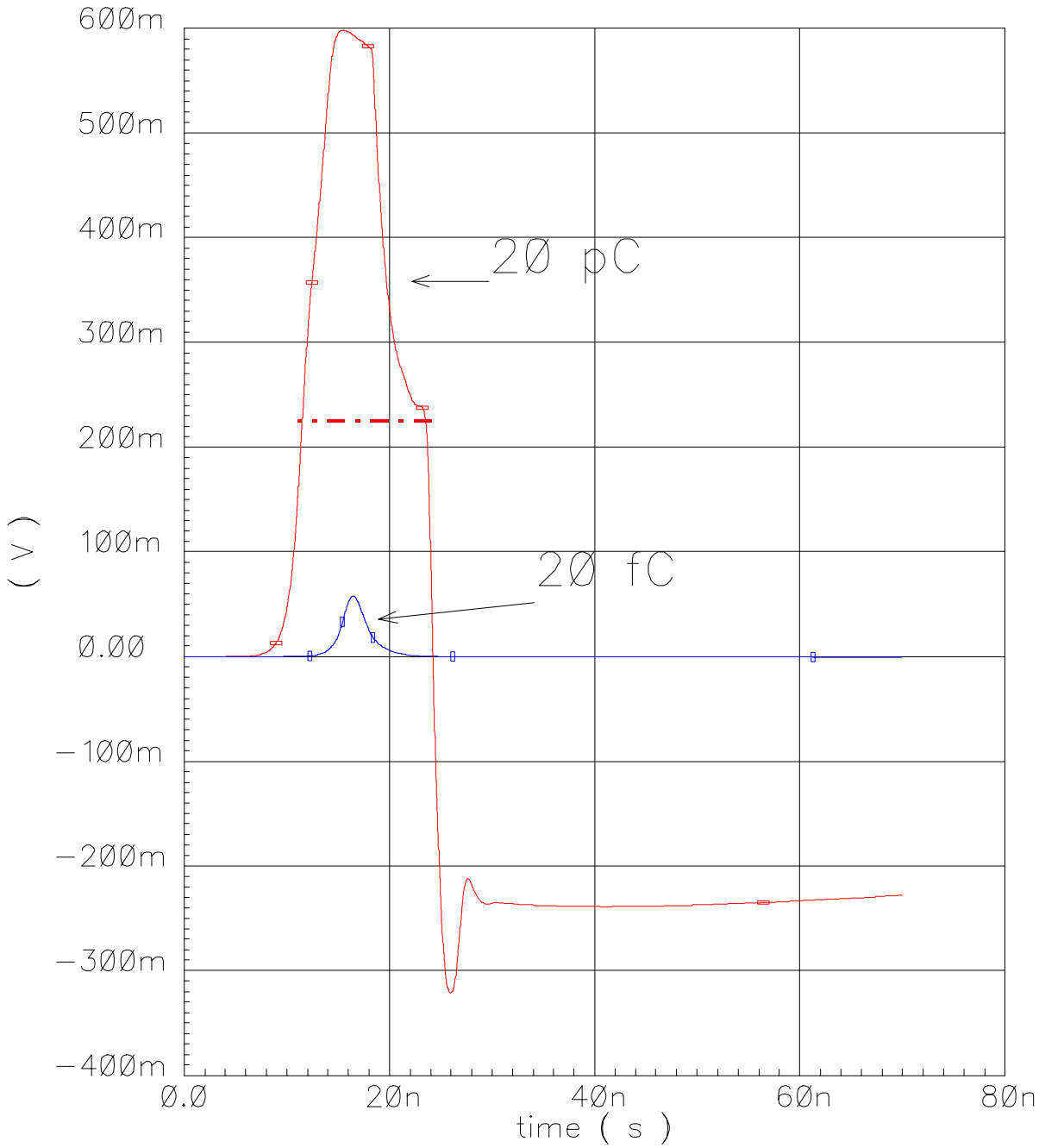
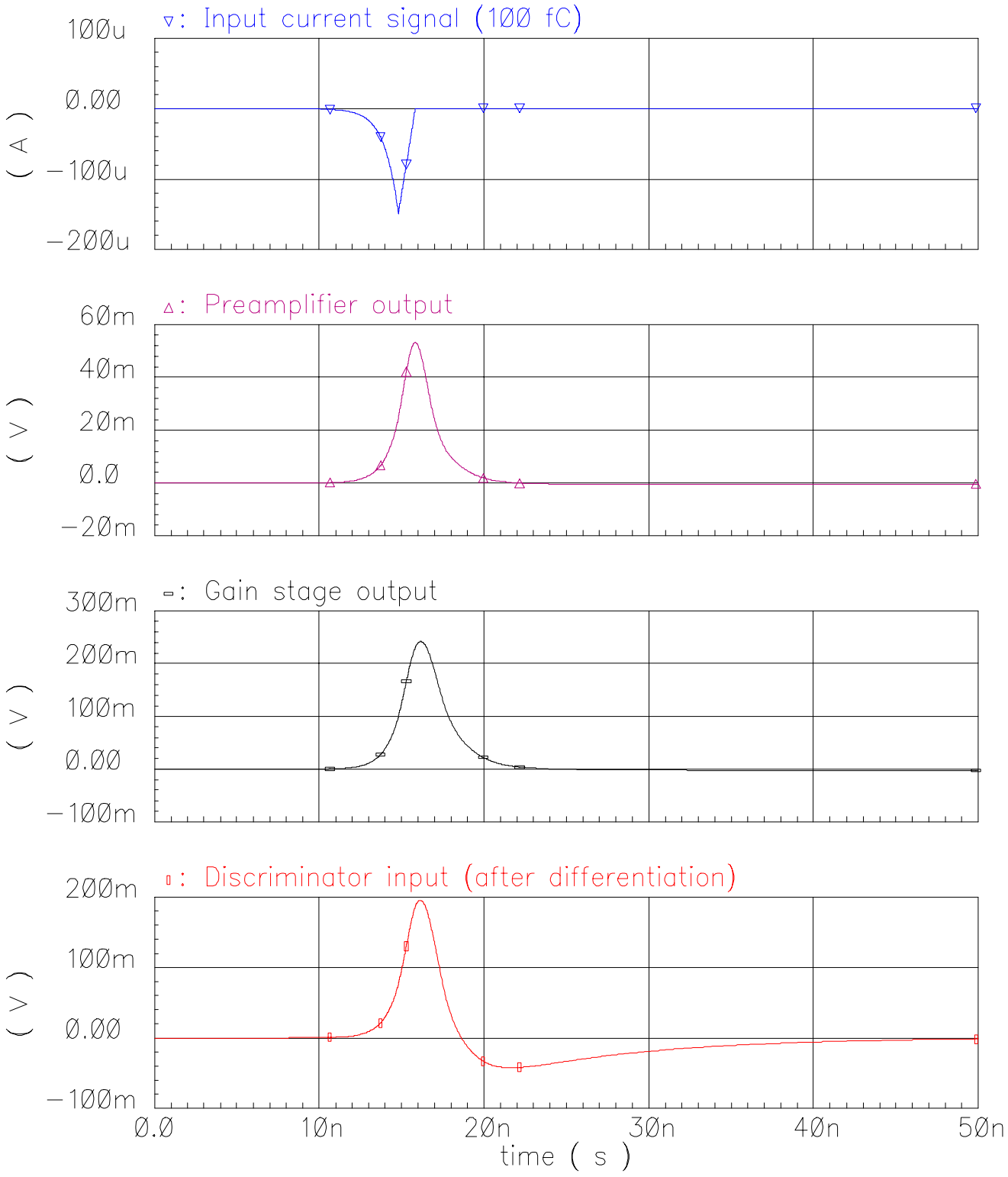
C-R differentiation produces a fast zero crossing

$$\sigma_{t\_n} = \frac{\sigma_n}{\left(dV / dt\right)} \quad \mathbf{t=t_0}$$

- **Overall charge sensitivity (up to 80 fC) ~ 2 mV/fC**
- **Bandwidth of Preamplifier-Gain stage: 90 MHz**

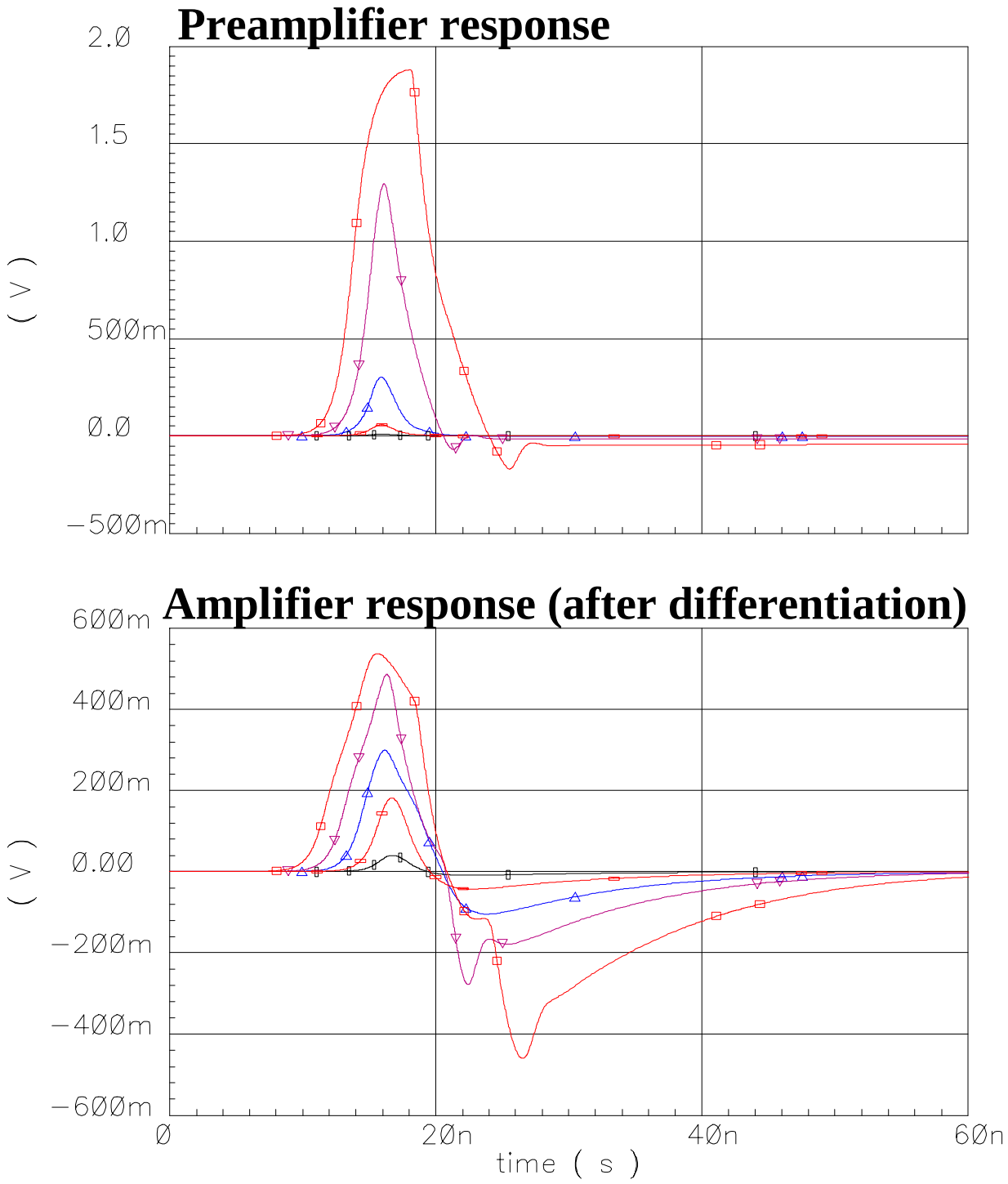


Gain stage: dynamic compression



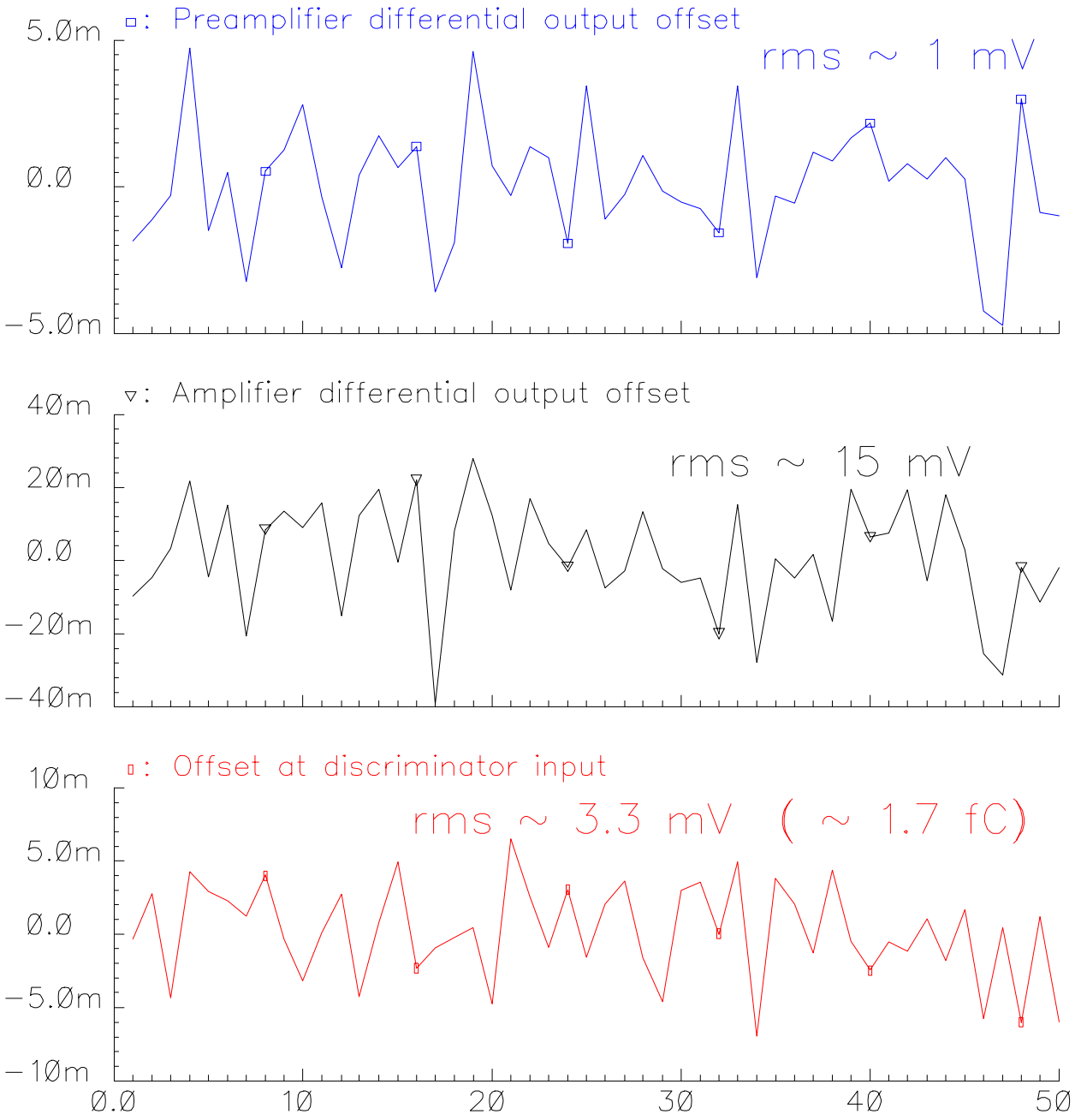
Typical transient response

20 fC < Qin < 20 pC



Typical transient response in the dynamic range

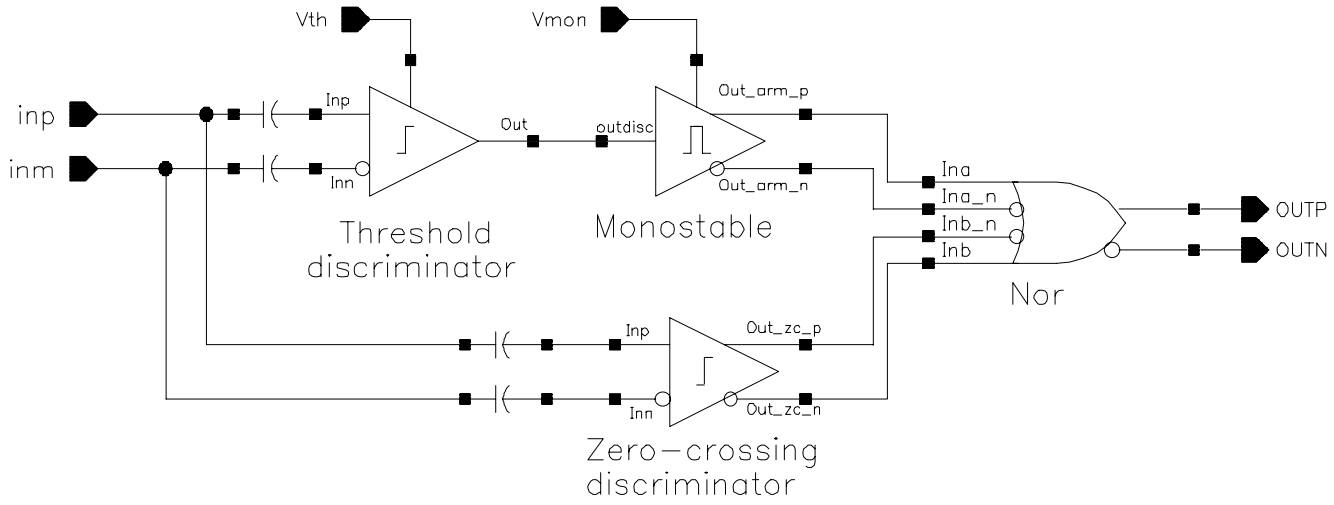
Monte Carlo Analysis



ZERO-CROSSING DISCRIMINATOR

- **Threshold discriminator**
- **Monostable (One-shot)**
- **Zero-crossing discriminator**
- **NOR**

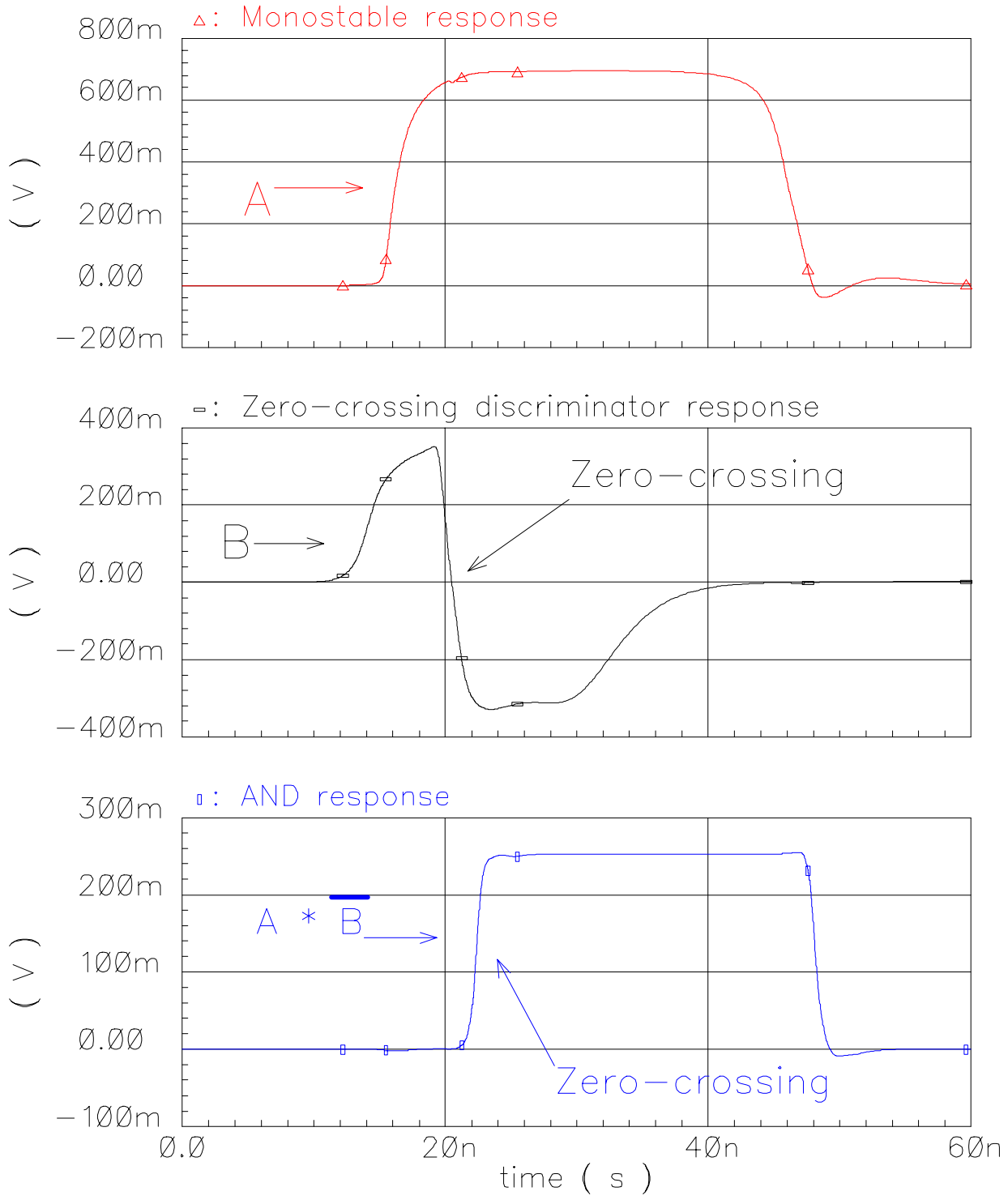
- **AC-coupling with amplifier (RC ~ 3 ns)**
- **50 ns ≤ T_{width} ≤ 400 ns**
- **Dead time ~ T_{width} + 10 ns**
- **f_{max} = 13 MHz (Qin = 2 pC)**
- **Power consumption: ~ 8 mW**



Zero-Crossing discriminator block diagram

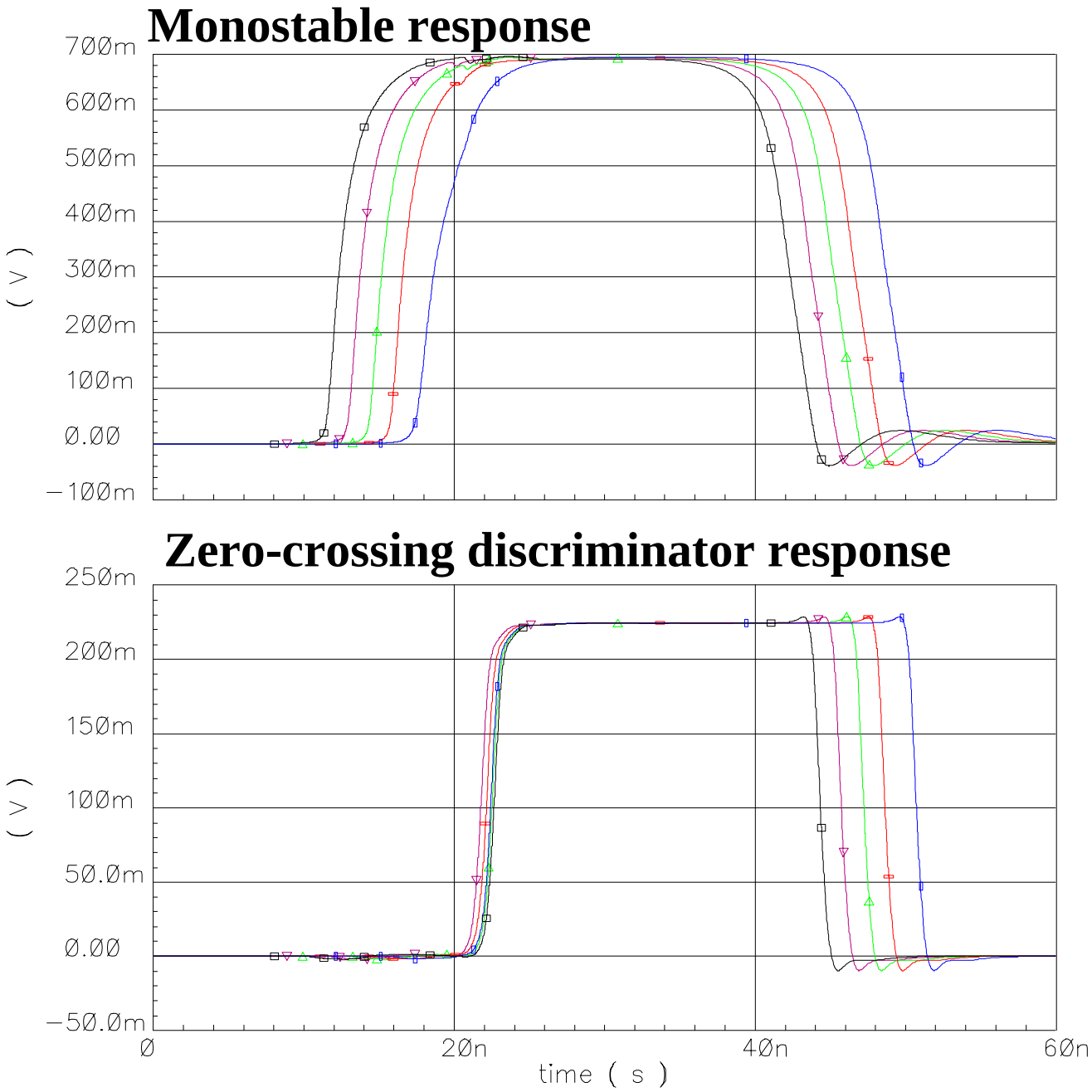
DISCRIMINATOR RESPONSE

Basic principles of operations



DISCRIMINATOR RESPONSE

1 fC < Q_{ov} < 20 pC



Discriminator output vs charge overdrive

DISCRIMINATOR RESPONSE

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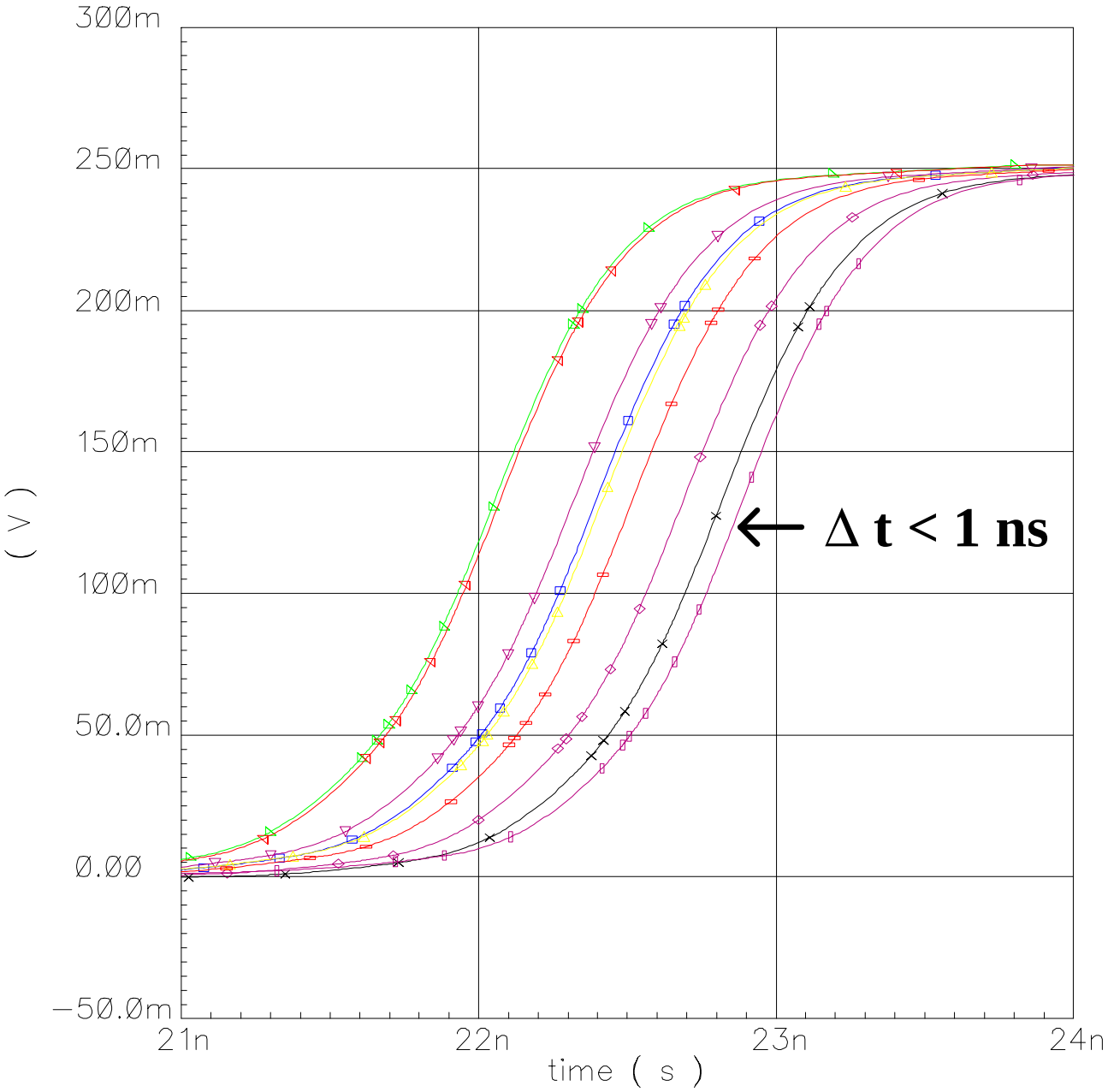
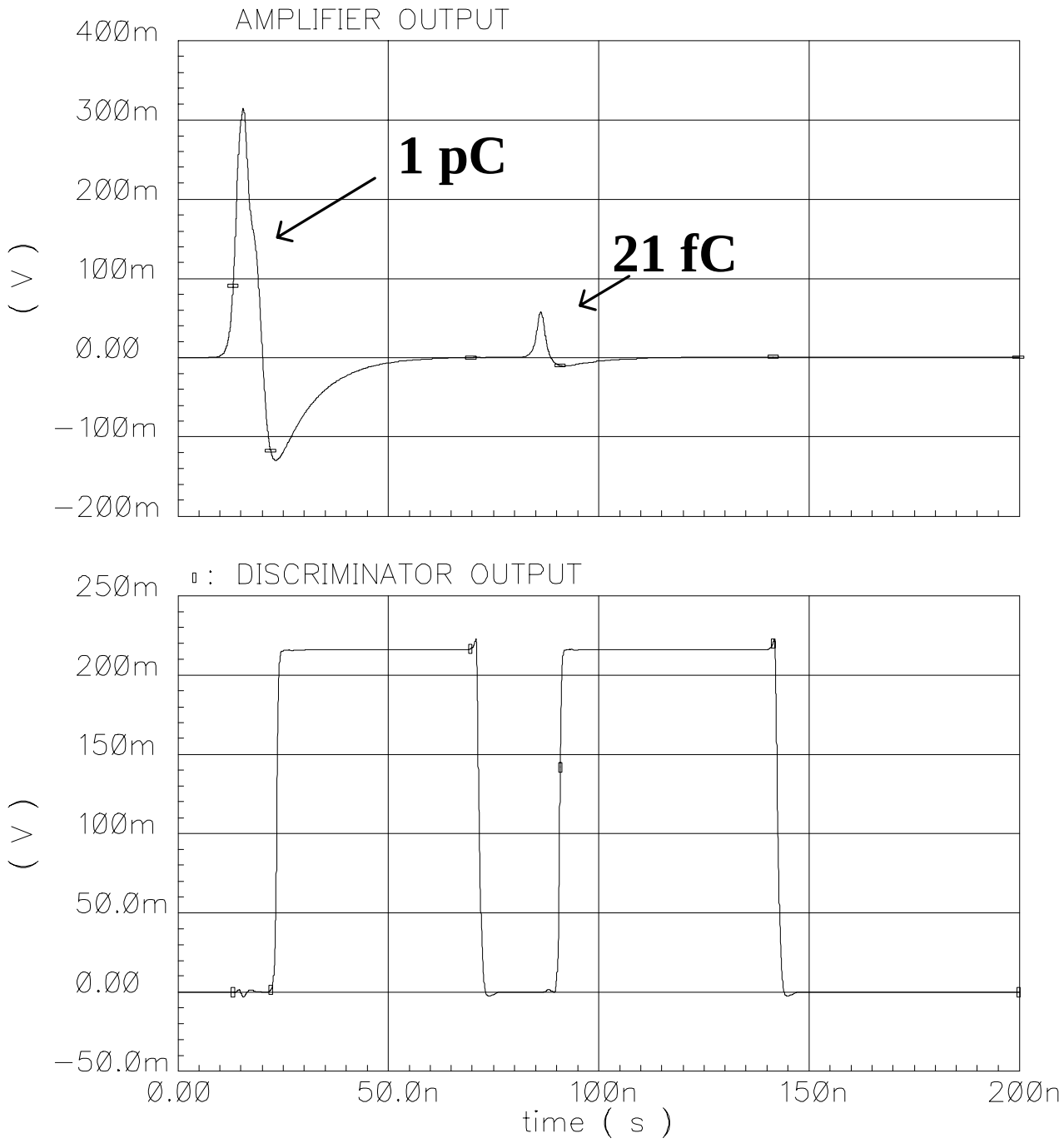


Discriminator output vs charge overdrive

DISCRIMINATOR RESPONSE

Double pulse resolution

Q_{th} = 20 fC

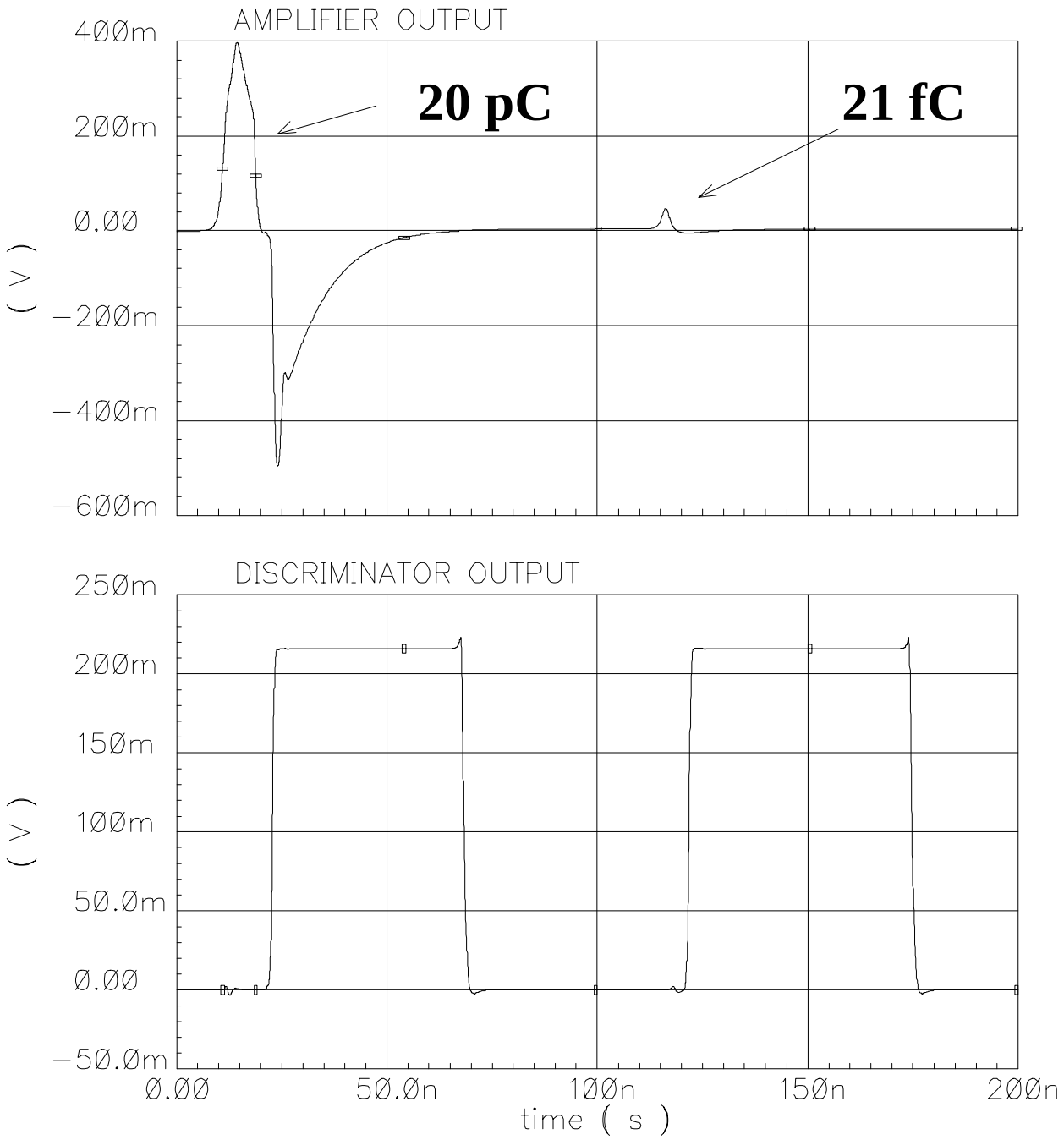


Dead time (typical case) ~ 70 ns

DISCRIMINATOR RESPONSE

Double pulse resolution

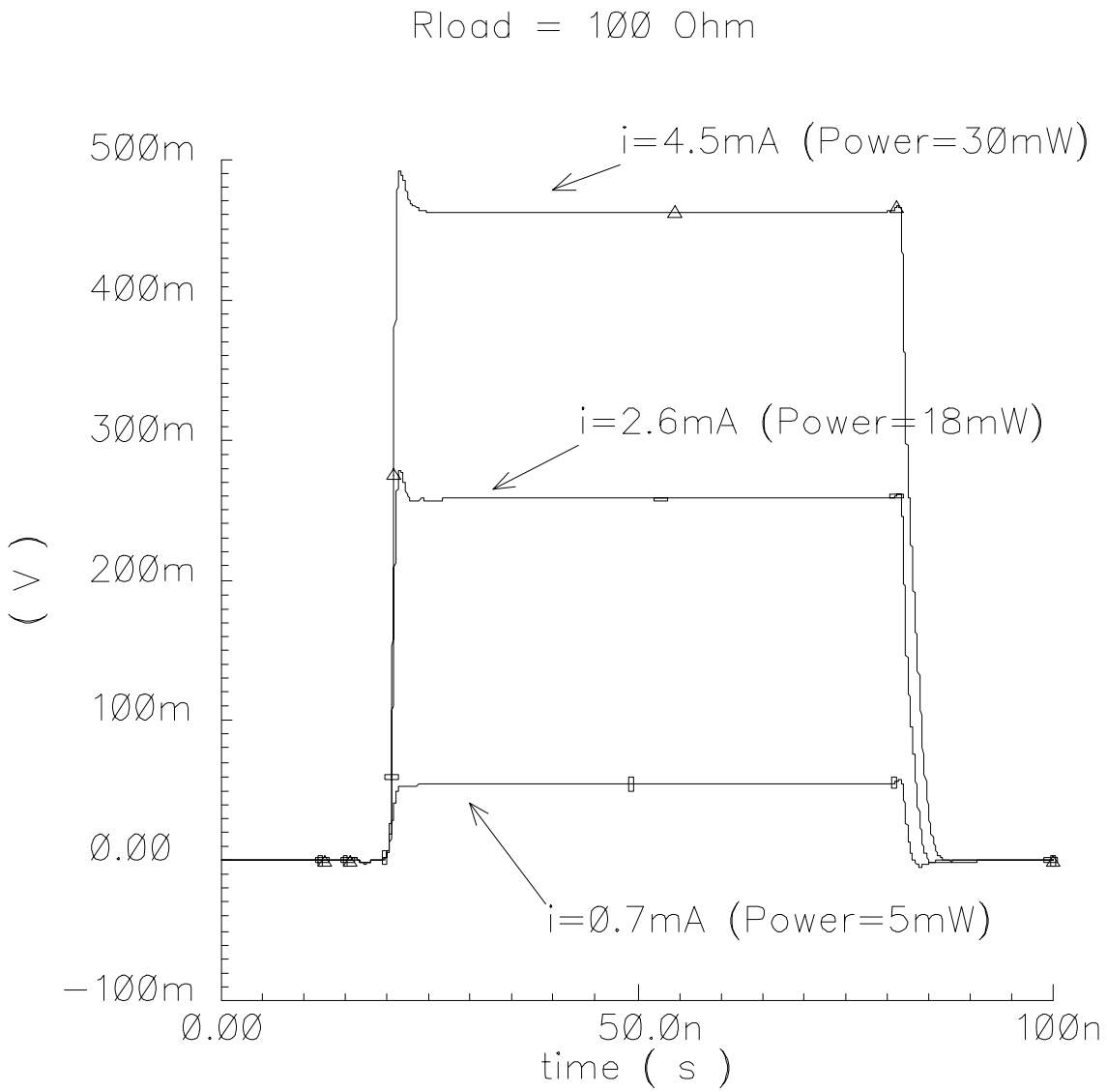
Q_{th} = 20 fC



Dead time (worst case) ~ 100 ns

OUTPUT DRIVER

- 110 Ω twisted pair cable
- LVDS receiver, 250 mV minimum signal
- Power consumption (typical): ~ 16 mW.



Output driver response

The output current is externally tunable and the power could be reduced down to 5 mW

CONCLUSIONS

- **According to the simulation results, this new chip fulfills to the requirements of the FE electronics of RPCs of CMS**

- **Design submitted on 30th november 1998 to CMP for prototyping**

- **We will receive 15 prototypes in March 1999**